White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements

Industry Council on ESD Target Levels

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Abstract

CDM has become the primary real world ESD event metric describing ESD charging and rapid discharge events in automated handling, manufacturing and assembly of IC devices. Its importance has dramatically increased in the last few years as package feature sizes, capacitance and pin count have scaled upward. In recent years, arbitrary CDM protection levels have been specified as IC qualification goals with little background information available on actual/realistic CDM event levels and the protection methods available in controls and device design for safe production of IC components. The rapid advancement of IC technology scaling, coupled with the increased demand for high speed circuit performance, are making it increasingly difficult to guarantee the commonly customer specified "500V" CDM specification. At the same time, the required static control methods available for production area CDM protection at each process step have not been fully outlined. Therefore, a realistic CDM specification target must be defined in terms of available and commonly practiced CDM control methods, and also must reflect current ESD design constraints. This is the scope of this White Paper II.

By balancing improved static control technology specific to CDM, and limited ESD design capability in today's leading technologies, we recommend a CDM specification target level of 250V. This is considered to be a realistic and safe CDM level for manufacturing and handling of today's products using basic CDM control methods.

At the same time we show that the current trend of silicon technology scaling will continue to place further restrictions on achievable CDM levels. It is therefore necessary that we present a realistic CDM roadmap for consideration by the industry moving forward to the next two levels of scaled technologies approaching 22nm and beyond.

About the Industry Council on ESD Target Levels

The Council was initiated in 2006 after several major U.S., European, and Asian semiconductor companies joined to determine and recommend ESD target levels. The goal was to set ESD requirements on IC products for safe handling and mounting in ESD protected areas while addressing the constraints from silicon technology scaling and IC design. The Council now consists of representatives from active full member companies and numerous associate members from various support companies. The total membership represents IC suppliers, contract manufacturers (CMs), ESD tester manufacturers, ESD consultants and ESD IP companies. *In terms of product shipped, the member IC manufacturing companies represent 8 of the top 10 companies, and 12 of the top 20 companies, and over 70% of the total volume of product shipped by the top 20 companies, as reported in the EE Times issue of August 6, 2007*. Membership on the Industry Council is continuously growing and interested parties should contact the Chairmen.

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Mission Statement

The mission of the Industry Council on ESD Target Levels is to review the ESD robustness requirements of modern IC products to allow safe handling and mounting in an ESD protected area. While accommodating both the capability of the manufacturing sites and the constraints posed by the downscaled process technologies on practical protection designs, the Council will provide a consolidated recommendation for the future ESD target levels. The Council Members and Associates will promote these recommended targets for adoption as company goals. Being an independent institution, the Council will present the results and supportive data to all interested standardization bodies.

Preface

This document was written with the intent to provide information for quality organizations in both semiconductor companies and their customers to assess and make decisions on safe ESD CDM level requirements. We will show through this document why a more realistic definition of the ESD CDM target levels for components is not only essential but is also urgent. The document is organized in different chapters with additional information in the appendices to give as many technical details as possible to support the purpose given in the abstract. We begin the paper with an Executive Summary and chapter / appendix highlights followed by Frequently Asked Questions (FAQ) so that the reader can readily find critical information without having to scan through the whole document. Additionally, these FAQ's are intended to avoid any misconceptions that commonly occur while interpreting the data and the conclusions herein. All component level ESD testing specified within this document adheres to the methods defined in the appropriate JEDEC and ANSI/ESDA as well as JEITA specifications.

Disclaimers

The Industry Council on ESD Target Levels is not affiliated with any standardization body and is not a working group sponsored by JEDEC, ESDA, JEITA, IEC, or AEC.

This document was compiled by recognized ESD experts from numerous semiconductor supplier companies and contract manufacturers. The data represents CDM and field failure information collected from a large variety and volume of IC products; no specific components are identified. The readers should not construe this information as evidence for unrelated field failures resulting from electrical overstress events or system level ESD incidents. The document only refers to component level ESD recommendations which should have no impact on system level ESD requirements.

The Industry Council, while providing these recommendations, does not assume any liability or obligations for parties who do not follow proper ESD control measures.

Glossary of Terms

AEC	Automotive Electronics Council
BGA	ball grid array
CBE	charged board event
CBM	charged board model
CCD	charged coupled device
CC-TLP	capacitively-coupled transmission line pulse
CDM	charged-device model
CM	contract manufacturer
CMOS	complementary metal-oxide semiconductor
CPM	charge plate monitor
DC	direct current
DIP	dual-in-line package
DRAM	dynamic random access memory
DSP	digital signal processor
DUT	device under test
DTSCR	diode triggered SCR
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EMS	electronic manufacturing supplier
EOS	electrical overstress
EPA	ESD protected area
ESD	electrostatic discharge
ESDA	Electrostatic Discharge Association; ESD Association
ESDS	electrostatic discharge sensitive
FA	failure analysis
FAR	failure analysis report
FCDM (FICDM)	field-induced charged device model
FCBM (FICBM)	field-induced charged board model
FIM	field induced model
FWHH	full width at half height
GND	negative voltage supply
HBM	human body model
HF	high frequency
HSS (HSSL)	high speed serial link
IC	integrated circuit
ICT	in circuit test
I/O	input/output
IEC	International Electrotechnical Commission
JEDEC	Joint Electronic Devices Engineering Council
JEITA	Japan Electronics and Information Technology Industries Association
LGA	land grid array
LNA	low noise amplifier
LV	low voltage
MCM	multichip module
MLF	micro leadframe package
MM	machine model

MV	medium voltage
NMOS	N-channel metal-oxide semiconductor
NPN	negative-positive-negative (transistor)
Node	Within a circuit, a point of interconnection between two or more components.
PCB	printed circuit board
PCTA	process capability and transition analysis
PMOS	P-channel metal-oxide semiconductor
QFP	quad flat pack
RC	resistor-capacitor network
RLC (LRC)	resistor-inductor-capacitor network
RF	radio frequency
SBLK	silicide blocked
SCR	silicon controlled rectifier
SDM	socketed device model
SERDES	serializer/deserializer transceiver that converts parallel data to serial data
SiP	system-in-package
SMT	surface mount technology
SoC	system-on-chip
TLP	transmission line pulse
TQFP	thin quad flat pack
ULSI	ultra large scale integration
VDD	positive voltage supply
Vds	drain/source voltage
VFTLP	very fast transmission line pulse
VSS	negative voltage supply
WCDM	wafer-level charged-device model
WSP	wafer scale package
ZIF	zero insertion force

ESD Design Window: The ESD protection design space for meeting a specific ESD target level while maintaining the required I/O performance parameters (such as leakage, capacitance, noise, etc.) at each subsequent advanced technology node.

ESD robustness: The capability of a device to withstand the required ESD-specification tests and still be fully functional.

I_{t2}: The current point where a transistor enters its second breakdown region under ESD pulse conditions and it is irreversibly damaged

Executive Summary

It is now well understood in the IC industry that the Charged Device Model (CDM) ESD is the ESD model which best describes real world component level ESD events during IC manufacturing and handling. See Chapter 1 for details. In contrast to HBM, where basic ESD control measures at the factory level ensure a single safe and realistic specification level (i.e. 1000V HBM as reported in White Paper I [1]), CDM protection requires additional degrees of ESD control such as managing against the charging of insulators, at specific process steps, to ensure safe and realistic levels for all product designs.

Some important aspects of the CDM challenge must be understood:

1. **IC Design / Development Constraints** which result from: **silicon technology scaling**, **IC high speed circuit design requirements**, and **larger IC package size trends**. See Chapter 2 for details. These constraints are inhibiting the ESD design methodology required to meet the commonly customer specified 500V CDM level. This is especially true for very high speed high performance pin design types, which have limitations in CDM discharge peak current. As a result, practical designs are restricted to 2-6 Amps of peak CDM current, which translates to a 200-400V CDM voltage level for many advanced technology products (depending on pin-count). Table I below contains representative cases that illustrate the peak current limitation for CDM protection based on high-speed pin design constraints, including the corresponding CDM voltage levels.

Table I: Advanced Circuit Design Impact on Achievable CDM Levels

Technology	Design Type	CDM Peak Current	Package Size	CDM Level
65nm	High Speed Serial Link	5-6 Amps	>300 Pins	300-400V
45nm	High Speed Serial Link	4-5 Amps	>300 Pins	250-300V
45nm	Radio Frequency (RF)	2-3 Amps	>200 Pins	200-250V

2. **Perceived CDM requirements** of 500V or greater. These no longer can be routinely met for the reasons discussed above, often leading to delays in qualification and time-to-market. The more important focus should be that the designs can no longer support these previous levels and that with the available CDM control methods there is no need for higher CDM levels that make the designs impossible for circuit performance.

3. **Improved state-of-the-art CDM ESD control** methods that are in practice in the industry today. These controls allow safe handling for devices with CDM pass voltage levels as low as 100V. This work has revealed several important findings that need to be considered before recommending a safe and practical CDM level.

A. Field returns data from 11 billion IC devices show that customer returns can occur for products with CDM pass levels from 200V to 2000V, meaning control

of CDM at production sites is more important than a specific performance target level. See Chapter 5.

B. Field failures also can occur when proper CDM control is not established during a product ramp-up (pre-qualification), meaning that production failures must be addressed by correcting the CDM control methods at critical process steps rather than requiring the designs to pass at higher voltages than are achievable by design. See Chapter 3.

C. CDM control measures are available throughout the industry to meet safe manufacturing and handling of products at 100V or above, meaning that products designed for CDM levels at 250V or 500V are equally safe and reliable with good margin. See Chapter 3.

D. Thus, any product with a CDM passing level of 250V or higher can be handled safely and reliably in a facility with basic CDM control measures. This level of protection should result in minimal impact on design and IC circuit performance requirements, and make them compatible with current technology trends. See Chapter 6.

E. As future IC technologies are enabled, there should be a continuous improvement of CDM control with even more advanced methods coming into practice.

4. Recommended CDM Levels: Based on this extensive study, a safe and practical CDM passing level of 250V is recommended at this time as outlined in Table II below. Products with a CDM level lower than 250V should implement additional process-specific measures for CDM control, especially during product ramp-up.

Table II: New Recommended CDM Classification Based on Factory CDM Control

CDM classification level (tested acc. to JEDEC)	**ESD control requirements**
$V_{CDM} \geq 250V$	• **Basic ESD control methods** with grounding of metallic machine parts and control of insulators
$125V \leq V_{CDM} < 250V$	• **Basic ESD control methods** with grounding of metallic machine parts and control of insulators + • **Process specific measures** to reduce the charging of the device **OR** to avoid a hard discharge (high resistive material in contact with the device leads).
$V_{CDM} < 125V$	• **Basic ESD control methods** with grounding of metallic machine parts and control of insulators + • **Process specific measures** to reduce the charging of the device **AND** to avoid a hard discharge (high resistive material in contact with the device leads) + • **Charging/discharging measurements at each process step**.

5. **Future Roadmap for continued silicon technology scaling.** As technology further scales towards the 22nm range and beyond, even this recommended 250V safe level will not be achievable by design due to impending further scaling effects and the drive towards higher circuit speed performance at data rates reaching 40 Gb/sec or more. We therefore envision that within the next five years, CDM levels into the 125V range would become the new practical targets as indicated in the roadmap of Figure 1. As a consequence, continuously improved CDM control and monitoring at the production areas must become a routine practice. Judging from the factory control methods and the expertise that are available today, this would not be and should not be an issue. As an important note, CDM control to 50V has already been successfully achieved in certain production areas. A continuous improvement in CDM control methods aimed at the 50V level as indicated below in Figure 1 is not only expected but is also imperative for future IC technologies.

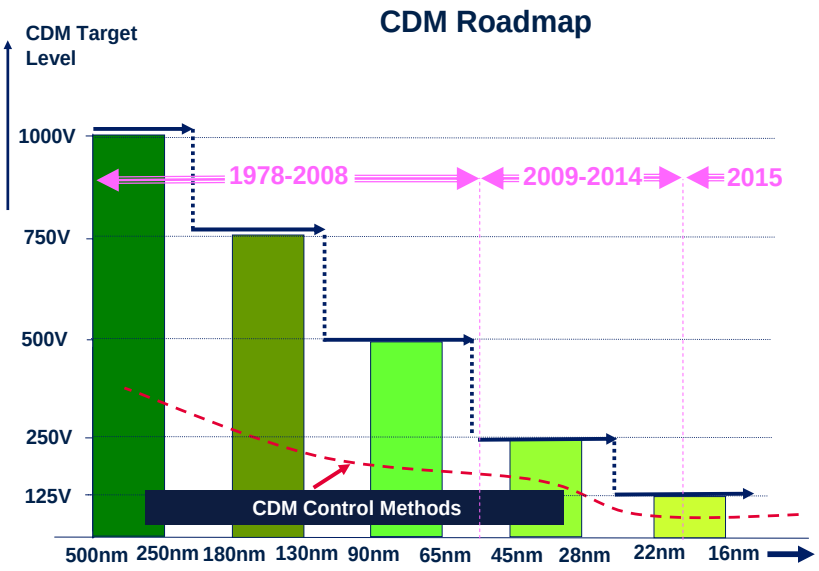

Figure 1: Technology scaling effects on practical CDM levels and the associated CDM control requirements

[1] White Paper 1: "A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements," August 2007, www.esdtargets.blogspot.com.

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Chapter Summary

Chapter 1: History of Charged Device Model since the initial 1974 publication is reviewed and major developments, mostly concerning CDM testers, are noted chronologically.

Chapter 2: This chapter outlines the protection design limitations associated with silicon technology scaling and the demand for high speed circuit performance. These protection design limitations become more pronounced with the trend for larger area, high pin count packages. With these constraints in view, the chapter points out the realistic CDM target levels that can be achieved in design today.

Chapter 3: The chapter describes two similar methods to analyze an assembly with respect to CDM risk and explains how to use these methods in actual production lines with examples. The field problems presented also show that if such a CDM risk analysis is not performed, even devices considered CDM robust may fail during assembly or testing, since the board can get charged and discharges with a higher discharge current than a single device at the same voltage level. A risk analysis performed following the described methodologies enables the manufacturer to handle even very CDM sensitive devices.

Chapter 4: A review of the current CDM goals for IC's from a manufacturer and customer view and the impacts that the current goals have on the manufacturer and end customer. The costs to the manufacturer of the current CDM target levels are highlighted in terms of design revision and time to market delay; the benefits of a new target level are similarly highlighted.

Chapter 5: The field return data of 11 billion shipped parts consolidated from numerous IC manufacturers are analyzed. The device types range from discretes to ULSI system-on-chip parts. Primarily field returns from the board manufacturers and end-customers have been considered. There is a weak dependence on the combined EOS and ESD failure return rate on CDM qualification level. In a data subset of 1.5 billion parts, it is demonstrated that EOS related fails (not CDM related fails) are dominating the failure statistics. Typical examples confirm that CDM related returns are usually caused by problems in the ramp-up phase of a manufacturing process. Minor yet critical changes in the ESD control of the manufacturing process solve these problems immediately as shown in Chapter 3.

Chapter 6: This chapter presents a total perspective on CDM control techniques available for production areas, and based on this recommends a realistic yet safe categorization of target levels which are linked to the required degree of CDM control methods. Considering all aspects from design capability to field reliability and combined with the currently practiced CDM control methods, it is proposed that a CDM level of 250V is a safe qualification target for now. As technology scales towards the 22nm technology and beyond, we envision that within the next five years CDM levels into the 125V range would become the new practical targets. As a consequence, continuously improved and monitored CDM control at the production areas must become a routine practice.

Appendix Summary

Appendix A: Simple circuit models can explain the major features of Charged Device Model (CDM) non-socketed ESD testers as specified by the ESD Association and JEDEC. A simple lumped series LRC model is estimated, and it explains features observable up to 1-2 GHz. This includes all major trends for peak current (Ipeak), which is plotted in the plane of effective L and C for a given value of spark resistance R. Extensions of this basic circuit model to a distributed one explain many reported high-frequency CDM effects.

Appendix B: A comparison between the CDM events in the real world and those in the tester world are presented along with descriptions of some typical cases. This chapter shows that the peak CDM discharge current from a high capacitance device in the real world is typically not as high as that in the tester world except on a power pin (bus).

Appendix C: This chapter describes existing CDM ESD test methods and standards and summarizes the differences between them. Weaknesses of existing test equipment and test methods are outlined. The chapter explains how these testing challenges can lead to inconsistencies and non-repeatability issues in product test results.

Appendix D: It is shown that no correlation of CDM to any other stress types (e.g. HBM, EOS and CBE) can be expected. Therefore CDM cannot be replaced by, nor replaces, any of the other stress types. Consequently, an increased CDM level will not lead to higher performance for other stress types

Appendix E: This chapter outlines charged board events (CBE) which result in damage to IC devices placed on printed circuit boards. The various charge / discharge mechanisms are described. Charged board events are higher energy counterparts to CDM for IC components, but different IC failure mechanisms result which do not correlate to other ESD event methods. A literature review is given along with techniques to evaluate CBE on systems. Recommendations to reduce CBE impact include improved ESD control and circuit board design / implementation guidelines.

Frequently Asked Questions

FAQ on CDM Qualification

Q1: Customers did not specify CDM levels before. Why are they asking for it now?

Answer: As the importance of HBM diminishes (even for units shipped below specification levels) as demonstrated by a lack of any field returns, customers are focusing more on CDM based field failure signatures, which are distinct from either HBM or MM.

Q2: If CDM methodology and levels are modified would there be more fallout for EOS at the component or System Level?

Answer: CDM and EOS failures are completely different in total energy and time duration. Effective CDM protection does not guarantee EOS protection. EOS protection must be provided at the system level. There is no correlation between component CDM failures and system EOS failures. The fallout rate due to EOS would not change as a result of modifying CDM methodology and levels.

Q3: As products with low CDM values have an increased risk for problems at introduction, shouldn't we aim for larger CDM levels?

Answer: Where 500V CDM can be achieved in design without degrading electrical performance or incurring additional product cost, this level of CDM should certainly continue to be implemented. However, Chapter 2 clearly shows that for several applications 500V is not feasible. Chapter 3 shows that solving the problems by CDM control measures is actually much more efficient than increasing the CDM robustness level at the cost of functional performance.

Q4: How is it determined that CDM levels lower than 500V are really safe?

Answer: It has been proven that even 100V CDM parts can safely be manufactured, if appropriate CDM control measures are taken (see Chapter 3). The assessment of ESD control measures and the field return data show that devices with 250V are equally as safe as 500V CDM parts in typical modern manufacturing sites.

Q5: When and where do classic CDM fails happen?

Answer: The classic CDM failure mechanism is a dielectric breakdown failure signature happening mainly in the ramp-up phase of a new product in the test area for a semiconductor manufacturer. This can also happen in PCB assembly lines or system assembly lines especially when new process steps are introduced.

Q6: If the new specifications are meant for all pins on a package, would it not make more sense to require higher levels for the corner pins?

Answer: With the automated pick and place tools today, any of the pins could make first contact. All of the pins need to be considered, the corner pins should not be treated any differently.

Q7: The council just made a case about lowering HBM levels. Will CDM levels follow automatically?

Answer: It has been shown that the HBM and CDM fail levels are largely uncorrelated. This is demonstrated in Appendix D, Section D.2. This is mainly due to the completely different physical discharge mechanisms and failure modes between the two models.

FAQ on CDM Control

Q8: If the production areas have basic controls for ESD would these methods also provide the necessary protection for CDM?

Answer: If the basic controls for ESD are in place and include controls for insulators, then the chances for ESD events of any kind would be minimized.

Q9: Many products that have been shipped at 300V, 200V, or even 100V CDM levels seem to be safe. Is it fair to say that CDM is well controlled with the basic methods or do they need special care for the 100-300V range?

Answer: With an ESD control program that addresses insulators and the charging of the device, handling of 100V CDM devices or higher should pose no threat.

Q10: What are the main weak points for CDM ESD control in manufacturing?

Answer: In contrast to controls for HBM, ESD controls for CDM rely on controlling the charge on insulators and controlling the discharge to the conductors of the manufactured devices.

Q11: Defining a maximum current level as a CDM target seems to be a good solution for the challenges with design of CDM ESD protection and also a good way to overcome the issues with variations in stress between different CDM testers and different CDM testing standards. However, how does a current level as the CDM target translate into a sensitivity level that is meaningful for the manufacturing environment?

Answer: While peak current makes sense from a device point of view, industry views sensitivity in terms of voltage. The experience both in the ESD control field and the qualification of devices is based on voltage values of the long-standing standards. Changing this to current would confuse both the end customer and contract manufacturers. The translation from the voltage level to current stays with the ESD protection designer. Knowing the product portfolio and typical packages, an estimate of the required withstand peak current can be made (see Chapter 2).

FAQ on CDM Requirements

Q12: Although your new target level recommendations seem to be valid from your analysis and from the collected data, our customers are not yet confident that our subcons have the measures to match the new requirements. How do we proceed?

Answer: By simply staying at the old levels, we will not address the design challenges which are discussed in Chapter 2. Additionally, it is the Industry Council's belief that customer demands for improved IO performance will only increase in the future, putting even more stress on the ability to achieve the current CDM target levels. Efforts to improve CDM protection in our manufacturing facilities needs to continue to be a focus area if we are to be prepared for these future challenges. As discussed in Chapter 3, basic CDM protection measures are implemented when the international standards are followed. The issue is that many are not aware of this as they do not perceive these measures as CDM protection measures. In addition to these basic CDM protection measures, an analysis of your production lines with the methods as described in Chapter 3 should be completed. This is especially true during the introduction of new process steps and during the production ramp-up phase as it has been found that CDM failures can occur for products with even higher CDM passing levels.

Q13: Chapter 1 covers highlights of CDM from the US and Europe, but does not mention the Far East. Weren't there some significant developments in Japan in the same time frame?

Answer: Yes, there were significant developments, and the authoritative summary is given as part of this White Paper work. The essentials are as follows:

1. The first CDM paper in Japan was presented in Electronics and Communication Conference with the title "Proposal of Charged Package Method", which influenced EIAJ Test Method IC121, Technical notes in 1988. Related EOS/ESD Symposium presentations from Japan were given in 1986, 1990, and 1992.
2. The EIAJ Semiconductor Reliability Sub-committee began standardizing CDM test methods in 1990; the Tentative CDM Test Method, EDX4702-01 was established in 1994.
3. The JEDEC Semiconductor Reliability Sub-committee (succeeding EIAJ Semiconductor Reliability Sub-committee) adopted EIAJ ED4701/300-2 (JEITA Standard) in April, 2006, aligning approximately with JESD22-C101D. The committee is now examining differences among the CDM specs and is looking for further improvements.

Q14: Our Company has a product in a MLF package which is planned to be sold as bare die or wafer level MLF. Will the CDM level change from package to die form, and how? Will the die have greater risk in assembly onto a board?

Answer: Bare die or wafer level MLF does show a higher peak current than the same die in a package, in most cases (particularly for packages containing only the die). If the die has the same connectivity to the board as the package (same or greater number of supply / ground connections), it could have a higher risk of charged board damage. Care must be taken to place the die away from insulators on the board which could charge up during assembly. See Chapter 3 and Appendix E.

Q15: With the roadmap shown for CDM, will there be a corresponding roadmap for HBM?

Answer: HBM levels are not package dependent and sufficient ESD controls exist in manufacturing to achieve 500V HBM today, so a roadmap for further reducing HBM levels is less necessary. This is explained in Chapter 2. Also, with today's modern packages with high pin counts, the HBM pin combination stress scenario in the real world is less meaningful. Therefore, CDM trends will be the most important and will dominate the achievable ESD levels.

FAQ on CDM Design

Q16: Why is the technology scaling such a severe issue for CDM design? If it is only related to gate oxide breakdown voltage limits, shouldn't the technology development engineers make the process more robust, since otherwise the transistors might get damaged during routine signal applications?

Answer: The gate oxide scaling continues for improved transistor performance. But it is about to reach a limit of tunneling effects and consequently the actual transistors are not easily damaged under normal circuit operating voltage conditions, which also scale. However, CDM stress does not scale and in fact gets worse for larger devices, and the breakdown voltage condition / charge trapping effects continue to take place at lower voltages. This results in the major challenges for CDM protection design.

Q17: Why are the designs facing such severe restrictions for CDM as opposed to HBM? Do you not use the same protection concepts?

Answer: While HBM designs also face restrictions as described in the White Paper 1, the impact on CDM is much harsher because of the relatively higher current levels involved in this stress test at levels close to spec targets. As a result a secondary stage protection is needed for additional voltage drops. But this secondary stage results in a drastic reduction in the high speed circuit performance and therefore the CDM design is a bigger challenge. The details are presented in Chapter 2.

Q18: If the design is such a critical issue for CDM performance is there an effort to develop more advanced protection concepts?

Answer: What we learned is that no matter which design is implemented, the fundamental nature of the capacitive loading and its impact on circuit speed does not change much. Some might claim that they have a more sophisticated design but eventually the physics of the limitations would take over.

Q19: Would the technology shrinks and the package size increases ever come to a saturation point such that a minimum CDM level would level off?

Answer: They could and most likely would. That is why we project a minimum CDM level of 50V could always be designed but this would depend on the eventual trends for circuit speed performance.

FAQ on CDM FAR

Q20: You claim in Chapter 5 that >1000V CDM cannot reliably be tested. Why do you include >1000V numbers in the analysis of Appendix D?

Answer: First of all many product datasheets state > 1000V performance. This is because the product sustained >1000V discharge. Appendix D details that such a stress is not always more severe than a stress at lower level. Secondly, Chapter 5 clearly shows that at those levels no dependence on the CDM level is observed. This supports the earlier remark.

Q21: Why did you choose to remove products with more than 100 fails?

Answer: The analysis of the FARs revealed that the statistics was dominated in all voltage classes by just a few designs showing EOS failure signatures. Therefore, these outliers have been removed to show that without them there is a relatively equal distribution across all classes with a failure rate below 1 dpm.

Q22: Is the connection between return rate and failure rate known for the studied population? Often, the customer does not return all failures and/or does not divulge the actual failure rates

Answer: Failure rate and return rate might not be equivalent in general. Typically the number of fails which get returned to the IC supplier is very high for automotive applications, while for consumer ICs customers there may not be as much interest in clarifying each fail. However, as also found in White Paper 1, the statistics of both consumer and automotive parts follow the same trend.

FAQ on CDM Test Methods

Q23: For CDM, is there a difference in the waveforms for inputs versus supply pins? Does this have an impact on qualification?

Answer: The CDM waveform is dominated by the capacitance between the device under test and the field plate. The total charge in the stress current is determined by this capacitance and is independent of the type of pin being stressed. Some difference in the waveform will occur due to differences in the impedance between inputs and supply pins. Comparisons of pulse shapes between ground, power and input pins on specific examples show that input pins have a slightly lower peak current and a slightly wider pulse width. The amount of peak reduction will vary from design to design. This difference in peak

current and pulse width is not a concern in qualification. Real world CDM events will be modified by the impedance of the stressed pin in the same way as in the CDM test.

Q24: How will the CDM tester variations be addressed?

Answer: The standards bodies are always reviewing the standards with the goal of improving them. The data presented in this white paper will provide these organizations with considerable data to aid them in improving the standards. However the standards bodies are encouraged to proceed with caution. The industry has considerable experience with today's test methods which gives users of the data a degree of confidence in the meaning of a particular pass or failure level. It is likely that any change in the standards to reduce variations will also produce a discontinuity in the measured CDM robustness levels. The standards bodies will therefore proceed with improvements cautiously.

Q25: Will the Industry Council address the Standards and tester variations in the future?

Answer: No. As stated previously, the Industry Council is not a standards body. We have set the recommended target levels based on the existing standards. Standard bodies have the responsibility to define physically consistent and practical standards. Test equipment vendors have the responsibility to produce testers that comply with the standards. Our conclusions in this document do not change any of these responsibilities. We do not at this time plan any work on coupling between the different standards.

Q26: Our Company is just starting CDM testing. Which CDM standard should we use for qualification and why?

Answer: All of the commonly used CDM standards address the same failure issues. The choice of the CDM standard may be best viewed as a business decision. If your primary customers are in the automotive industry, the best choice is the ESDA/AEC method. In the more general electronics industry the JEDEC standard may be a better choice. Many companies have found that they need to maintain the capability to do either standard, depending on customer demand. Fortunately the ESDA/AEC and JEDEC test methods can be done on the same tester, requiring only the change of test heads and the use of different calibration modules. If a large portion of your business is in Japan it may be necessary to use the JEITA method. Unfortunately most CDM testers do not support all three standards.

Q27: If our Company has a 500V CDM part with the JEDEC test method, what does this mean for the ESDA/AEC method?

Answer: A part with a 500V CDM level when tested with the JEDEC test method will likely have a lower failure threshold if tested with the ESDA/AEC method due to the generally higher current levels produced in the ESDA/AEC method for the same voltage. Unfortunately it is not possible to apply a strict scaling law between the two test methods. Differences in the geometry between the two test methods make it likely that different package types will scale differently between the two test methods. See Appendix C.2 for additional information.

Q28: If our company has a 500V CDM part with JEDEC test method, what does this mean for the JEITA method?

Answer: A 500V JEDEC CDM part will likely pass at a higher voltage with the JEITA test due to the lower currents in the JEITA standard for the same voltage. Similar to the ESDA/AEC to JEDEC comparison, it is not possible to strictly scale the passing voltage between the two test methods. See Appendix C.2 for additional information.

Q29: Why are there three different CDM standards? Is there a customer perception of differing performance of one model over another? Which features of the CDM environment require three different standards?

Answer: The existence of three CDM standards is largely due to differing organizational structures and history and not due to an effort to model a different physical mechanism. It is true that some people have a preference for one standard over another. It may be due to a preference for one calibration method over another or a preference over how one standard explains the measurement procedure. Often it is due to familiarity. Use of a particular test method for an extended period of time will bring a level of confidence in the results. A change to a different test method will require a rebuilding of confidence.

Q30: If the IC device fails CDM due to charge / rapid discharge, shouldn't the charge on the device be included in a CDM metric?

Answer: Charge is certainly an important quantity in the CDM test method. The CDM test method, however, is built on the assumption that different integrated circuits will charge to similar voltages if handled in the same way, without regard to the size of the integrated circuit. The amount of charge needed to reach a particular voltage will scale with the capacitance of the circuit to its surroundings. If the capacitance of the device to the field plate is known it is then straight forward to calculate the charge on the device. This charge will relate to the size of the current pulse and therefore has a bearing on the protection design required for a particular size device.

FAQ on Charged Board Events and EOS

Q31: Are Charged Board events (CBE) related to CDM and hence the IC pins should really be designed to CBE?

Answer: The CBE discharge mechanism is conceptually related to CDM for a single component. However, the board level aspect of CBE (much greater capacitance of supply/ground planes and reduced inductance of the supply/ground path) makes the CBE failures much more severe in comparison with CDM. They are easily mistaken for EOS. Component IC pin ESD protection cannot be designed to protect against CBE, which can be quite large and can vary considerably from application to application. Additional system level EOS protection must be provided. See Appendix E.

Q32: If CDM methodology and levels are modified would there be more fallout for EOS at the component or System Level?

Answer: CDM and EOS failures are completely different in total energy and time duration. Effective CDM protection does not guarantee EOS protection. EOS protection must be provided at the system level. There is no correlation between component CDM failures and system EOS failures. Please refer to Appendix D.1 and Appendix D.1.3 for details. The fallout rate due to EOS would not change as a result of modifying CDM methodology and levels.

Q33: Can CDM replace or be replaced by any of the other ESD standards?

Answer: No. The energy, time duration and nature of the discharge are so different that CDM is complementary to the other standards. Appendix D addresses this question.

Q34: I often hear that the IEC61000-4-2 pulse is a superposition of a CDM and a HBM pulse. Can IEC61000-4-2 ESD testing replace CDM and HBM testing?

Answer: No. Looking at the two peaks in a 61000-4-2 pulse the time duration is indeed comparable to a CDM and HBM pulse. However the required levels and discharge nature are completely different. This is because the CDM is intended for component level testing and the IEC61000-4-2 is intended for system level testing. See Appendix D, Sections D.1 and D.1.2. for details.

FAQ on CDM Phenomena

Q35: How does CDM discharge occur in the real world or in the factory?

Answer: CDM discharge occurs when the voltage difference between a charged device and other metal body exceeds the breakdown voltage of the small air gap between them. If the voltage difference is high, discharge begins at a wider gap distance and spark resistance is higher. If the voltage difference is lower, discharge does not occur until the gap distance becomes small enough and spark resistance is lower. See Appendix B for more detail.

Q36: Why and how is the device statically charged?

Answer: E-Field charging and tribocharging are the main methods of device_charging. Changes in the electric field around a device change the potential of the device without changing the net charge on the device. The change in potential makes the device vulnerable to a rapid current pulse or CDM event when it contacts a conductor at a different potential. Tribocharging occurs if a device slides across the surface of another object. Other examples of tribocharging are picking up a device from a tray or carrier tape and peeling of a cover sheet or tape from a tray or reel. See Appendix B, Section B.1.2.

Q37: Does CDM stress in the real world depend on the device package?

Answer: CDM stress in the real world is changed by the device package and many other conditions such as relative humidity, temperature, contact surface, and contact speed. The package is the major part that defines the capacitance of the charged device and the capacitance of the discharging object, as well as affecting the inductance and resistance of the discharge path. The package type also decides the handling method in the manufacturing environment that is most likely to cause the charging and discharging effects. More details are given in Appendix B.

Q38: What are major differences between real world CDM and tester world CDM?

Answer: The purpose of tester world CDM is to give the most stable and repeatable charging and discharging of the device, because it is a qualification tool. The tester keeps parameters such as charging voltage, device charging capacitance, contact speed, device discharging capacitance and discharging resistance as repeatable as possible. Discharging inductance should be reasonably low to meet the requirements of the test standard. In real world CDM events, on the other hand, most of these parameters cannot be easily controlled. The only thing one can do is to eliminate operations that charge or discharge a device or reduce the charge on a device. In the real world, device capacitance at charging and discharging is typically very different (capacitance at charging << capacitance at discharging). More details are given in Appendix B.

Q39: How do I use the analysis of Appendix A to calculate the now-familiar plots of I_{peak} vs. package size, or of I_{peak} vs. effective capacitance?

Answer: Start with the simple 3-capacitor model in Appendix A.1. Package dimensions, plus probe lengths, dielectric properties, and other features of the CDM machine are sufficient to calculate the three capacitances and solve the network to give the effective capacitance C_{eff}. This can be set up on a spreadsheet with the variables easily controlled. Larger package size will make for a larger C_f and C_g, but will subtract from C_{frg}. Fringing fields always enter in but their effect can be estimated easily enough. Notice that as package size grows, the C_{eff} will grow sub linearly due to the limiting effect of C_{frg}, which depends on field plate, upper ground plate, and actually declines with package size as noted above.

Once you have a C_{eff} for the package, the inductance values L_p and L_d can be estimated from Table A-I for the simple 2-pole model (i.e., forget C_d and C_p) and the I_{peak} expression(s) can be used to calculate I_{peak}. Again, this is easily captured in a spreadsheet. A resistance, R, of 25 ohms for the ESDA or JEDEC CDM machine spark fits well in most comparisons to measured data. In most cases $R<2\sqrt{(L/C)}$, so you will use the inverse tangent expression, underdamped (i.e. Equation 9b). Remembering the relation between package size and C_{eff} for a particular package design and presumed inductance values, you can now plot I_{peak} vs. package size, or C_{eff} as measured by charge in the CDM pulse. It is evident from Figure A7 in Appendix A that I_{peak} goes up as C_{eff} goes up, although the increase is sub linear, as expected.

Q40: Can the analysis of Appendix A also be used to find the effect of package trace length on peak current?

Answer: Yes. This is only a little more subtle than I_{peak} vs. package size or C_{eff}. Once C_{eff} is determined for a particular package, package trace length affects the inductance, as the package trace behaves like a nearly-shorted transmission line of a particular length. Table A-I in Appendix A gives an approximation of the inductance, L_d, of package traces of various lengths. These inductances are added to the L_p values in Table A-I for the test head, giving a total inductance for the simple 2-pole model. Again, for that model we must overlook distributed capacitance C_p and C_d, but that can be done if you're looking for a simple waveform and a single I_{peak}. Figure A7 again is helpful, and it is clear that I_{peak} goes down as total inductance goes up, with trace length being some fraction of that total inductance.

Chapter 1: CDM Background and History

Timothy Maloney, Intel Corporation

Since the 1970s, Charged Device Model (CDM) has been associated with mechanical handling of integrated circuits (ICs) and is cited as a reason for failure of those ICs. Much of the early work was done at Bell Laboratories [1, 2]. Some of this very useful early work at Bell used a simple vacuum relay to switch stored charge from a component to a nearby ground plane. This was simple but effective, and allowed many designers (at many locations, due to Bell's willingness to talk and write about it) to improve their semiconductor components. Bell continued its work on CDM in the late 1980s and early 1990s in their development of a machine [3, 4] that evolved into the commercial testers of today. These CDM testers are usually built to be in agreement with CDM test standards by the ESD Association and JEDEC [5,6], first released in the mid-1990s. We will call these CDM testers ns-CDM or non-socketed CDM testers.

Components become charged during handling because of triboelectrification or because of being moved into the region of an electric field. Triboelectric charging results from frictional contact by dissimilar materials, while E-field induction takes place near a surface (e.g., nonconductive plastic) that is already charged. CDM ESD stress results when a component under such influence connects to an equipotential surface (e.g., a pin touching grounded metal in a socket). For either the triboelectric or the E-field charging, the effective component area figures heavily in the total amount of CDM charge. For triboelectricity, charge is expected to be proportional to the interfacial contact area with the other surface, while for E-fields, Gauss' Law (normal E-field proportional to surface charge per unit area) indicates that charge goes as component area.

The Bell Labs CDM tester [3,4] for semiconductor components, a non-socketed CDM tester, was developed in order to duplicate real CDM events as closely as possible. These machines were set up so that the CDM stress depends on the semiconductor package being used, the charge scales with package area, and so on. The standards adopted by ESDA and JEDEC [5,6] allow a field-induced CDM test system, so called because it literally uses a field plate to induce charge flow on and off the component. Figure 2 is a sketch of the ns-CDM tester from several Bell publications that was reproduced in the JEDEC CDM spec. This method is basically equivalent to the direct charging CDM method, whereby a single pin (usually a substrate pin) charges the device with respect to a ground plane located under the dielectric, and the CDM discharge is applied with the discharge probe. The ESDA CDM spec [5] allows for both direct charging and field-induced test methods, with several commercial versions of the tester allowing for both kinds of CDM testing. Figure 3 shows a CDM waveform as sketched in a CDM standards document, in this case JEDEC.

Since the early 1990s, the Socketed Device Model (SDM) has been a convenient way to exploit automated ESD testing equipment for CDM-like testing of components, using sockets and relays. The history of the first full decade of SDM testing is well reviewed in a 2001 article [7], which followed shortly after the ESD Association technical report on SDM [8]. Waveforms and parasitics associated with SDM were found to be very different from ns-CDM, although both had the fast-pulse character of CDM and were useful in

discerning product weaknesses to CDM. But the advances in process technology of the 1990s, along with much testing of components, made it clear that SDM and ns-CDM could not be unified into one standard.

A brief history of CDM developments is as follows [9]:

- 1974: Model was first proposed by Speakman —"Human body model is not the only concern to semiconductor users".
- 1980: Bossard et al — "ESD damage from triboelectrically charged pins". Details of the potentially damaging model were given in this paper.
- 1985 and 1986: British Telecom workers made experimental investigations of the field induced ESD model.
- 1985 and 1986: With the rapid introduction of automated handlers, CDM has become a major ESD failure mode.
- 1986: Japanese reported the first automated CDM testing system. (Fukuda et al, OKI Electronics)
- 1987: Siemens Group reported susceptibility of 256K DRAMs to the CDM testing versus real world situations.
- 1987: Avery (RCA) reported design techniques for CDM protection.
- 1988: Maloney (Intel) reported more extensive design guidelines to avoid CDM failures.
- 1989: AT&T reported a field induced charged device model simulator.
- 1995-Present: CDM failures became an important issue for IC devices with the shrinking of gate oxide thickness.

Much of this history was discussed in a recent review article about CDM [10].

In the initial stages of work on CDM and through the 1980s, the most common target voltage for CDM performance was 1500V. This was usually achievable with the equipment used and was achievable for the semiconductor devices. For relay-based methods, passing 1500V tended to compensate for the slow rise time and reduced peak currents of a relay-based system. However, as the testing hardware advanced, along with advances in semiconductor technology and our knowledge of what the components really experienced, opinions about the voltage target changed and lower voltage targets were accepted. The ns-CDM tester became better understood in terms of its actual rise time, peak currents and waveform shapes and users built up confidence in its ability to reproduce factory-level events. At present, 500V has become acceptable to most of the industry as a ns-CDM voltage target for components that will be handled under "reasonable" static control conditions. A recent study of CDM stress in the factory and how it relates to the ns-CDM test voltage scale has revealed that 500V ns-CDM performance should usually meet those expectations comfortably [10].

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[10] T.J. Maloney, "CDM Protection, Testing and Factory Monitoring is Easier Than You Think", 2007 Taiwan ESD Conference Proceedings, pp. 2-8 (invited keynote speech and paper).

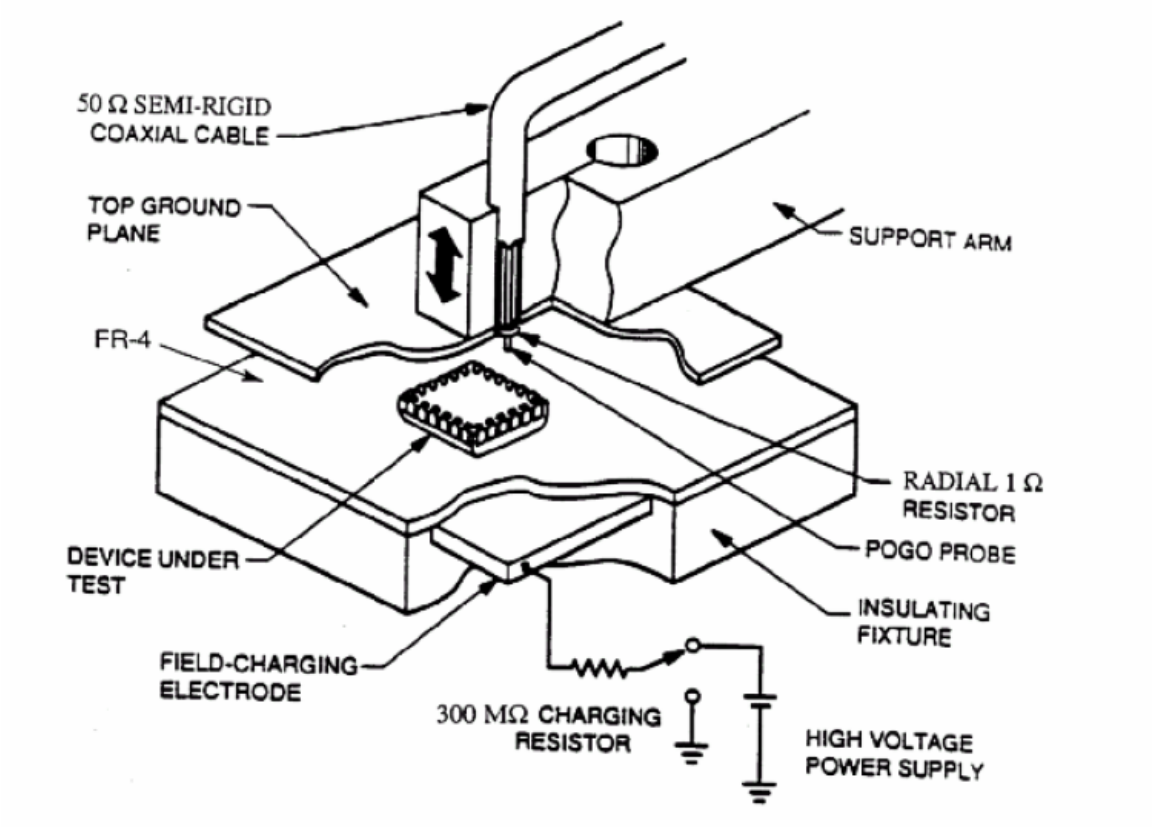

Figure 2: Sketch of ns-CDM charge device model test system by Bell Labs and incorporated in JEDEC CDM specification.

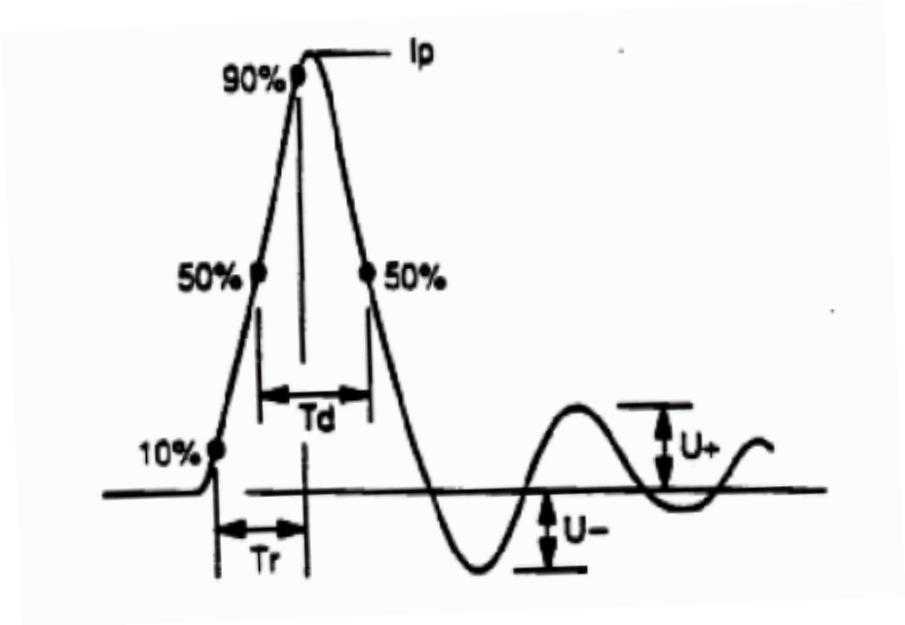

Figure 3: CDM waveform from ns-CDM standard document. Td is about 1 nanosecond.

Chapter 2: CDM Challenges to IC Component ESD Design

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James W. Miller, Freescale Semiconductor
Robert Gauthier, IBM

2.0 Introduction

Over the past decade, Charged Device Model ESD testing has increasingly become an industry requirement for qualification of IC components. Unfortunately, over this same time interval, three trends have combined to greatly complicate the task of designing effective on-chip CDM ESD protection circuits.

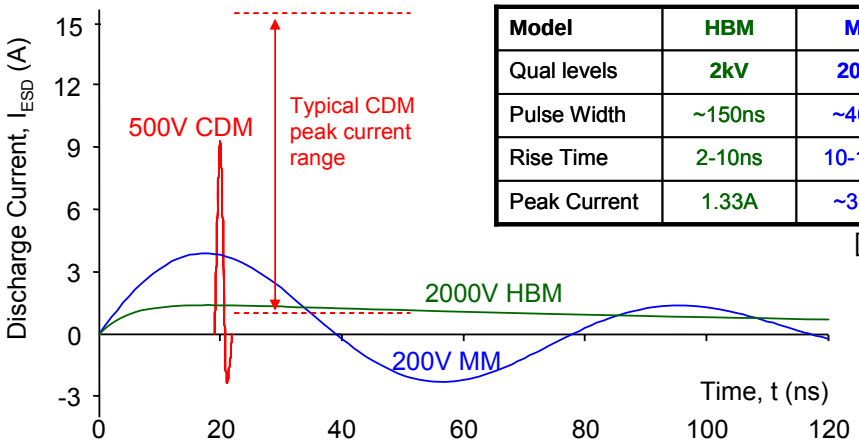
1. The pin count and size range of IC components has grown significantly. This is a serious issue because the peak current produced during CDM testing at a given pre-charge voltage is a sensitive function of die and especially package size. The net result is that the upper range of CDM currents seen on products is increasing rapidly. Large increases in ESD layout area on the die are required to protect fragile circuits at these higher currents. In some cases the required ESD layout area becomes prohibitively large.
2. Advancements in IC process technologies with smaller and more fragile active devices as well as thinner and more resistive interconnects have degraded the ESD robustness of circuitry to be protected. This makes it more difficult to protect the component at a given CDM current level.
3. Mixed signal ICs with high speed digital, RF analog and other performance sensitive pins are becoming much more prevalent. Strict electrical performance limitations on these pins limit options for ESD protection. This often makes it impossible to meet typical CDM ESD qualification criteria.

Taken together, these trends have led to greatly increased challenges for the design of on-chip ESD protection. As a result, many new products today fail or are marginal to the most common CDM qualification target of 500V. This is a fundamental problem that will only get worse as these trends continue. This chapter is an attempt to summarize the CDM challenges to IC component ESD design presented by these continuing trends.

2.1 The CDM Event from the ESD Designer's Perspective

As described in Appendix A, the CDM ESD test differs considerably from the HBM and MM tests, both in terms of the tester configuration and the current waveforms produced. These waveforms are compared in Figure 4 [1]. Both the HBM and MM tests utilize a socketed DUT, with the stress pulse delivered between one or more stressed and grounded pins via an external pulse source. The resistor-capacitor (RC) network used in these sources produces relatively long pulse widths of ~40ns for MM and ~150ns for HBM. For both MM and HBM, the peak ESD current at a given pre-charge voltage is more or less fixed, independent of the DUT. In contrast, during the non-socketed CDM test, charge is distributed over the entire DUT and flows through multiple paths to a

single grounded pin. Important consequences of this configuration are that the resulting pulse width is very short (~1ns) and that the peak current produced can vary widely from DUT to DUT, depending on die and package size. As can be seen in Figure 4, CDM current amplitudes typically vary in a large range from 1-16A. Note that, at the 16A upper limit shown, the 500V CDM peak current exceeds that of a 2000V HBM event by approximately 12X, and that of a 200V MM event by 4.4X.



Model	HBM	MM	CDM
Qual levels	2kV	200V	500V
Pulse Width	~150ns	~40ns	~1ns
Rise Time	2-10ns	10-15ns	100-500ps
Peak Current	1.33A	~3.6A	1-16A

[Gieser] (modified)

Figure 4: Comparison of current waveforms for CDM, MM, and HBM ESD events.

While component ESD stress levels are typically defined in terms of a stress voltage (i.e. 2000V HBM or 500V CDM), these voltage values are largely meaningless to the ESD designer. Designers consider the ESD event in terms of the resulting current waveform. Elements in ESD protection circuits and ESD conduction paths are sized based on a target peak stress current and duration. In general, if the target peak current increases, the ESD elements and conduction paths must be increased in size accordingly. In fact, as will be shown below, ESD layout area on the IC increases not linearly, but exponentially with increasing CDM peak current targets.

Another challenge which is unique to CDM is the fact that the true peak current is not known until each new packaged component is tested. When designing, for example, ESD protection for an I/O cell library which may be used in a wide range of products, the designer is forced to estimate peak CDM currents based on the estimated capacitance of the largest expected die and package. Accurate capacitance information is often not available, forcing the ESD designer to more or less guess a CDM peak current target for the I/O cell library. Marginal component CDM ESD performance is often a result of inaccurate capacitance estimates in the ESD design phase of I/O cell library design. Furthermore, if a given product design changes to a newer larger IC package, surprisingly lower CDM performance may result.

2.2 Design Techniques for CDM

In advanced CMOS technologies, circuitry which connects directly to Input/Output (I/O) pads are often most at risk of damage during a CDM ESD event. In this section, two very

common approaches for protecting I/O circuitry are briefly described. This will provide a framework for describing CDM ESD protection challenges in the following sections.

2.2.1 Double Diode ESD Protection

A schematic of a dual diode I/O ESD protection strategy is shown in Figure 5 [2-6]. The I/O pad connects to receiver and driver circuitry which are powered by the Vddx and GND supply buses. Both primary and secondary ESD protection elements are placed to protect receiver transistors M1-M2 and driver transistors M3-M4, which are typically the I/O devices at greatest risk during ESD. Consider the case where the I/O pad is grounded during a negative CDM event. Most of the positive current will follow a primary path from the grounded I/O pad through the forward biased D1 diode to the Vddx bus, then down the ESD power clamp to the GND bus, and then from the GND bus metal grid throughout the rest of the IC and package. Note that it is important to minimize the total voltage drop between I/O pad and GND bus local to the stressed I/O pad during this ESD event. Diode D1 and associated interconnects must be adequately sized. It is also important to minimize parasitic Rvddx and Rgnd bus resistances, since they add to the total voltage drop along this primary ESD current path. To better protect large banks of I/O cells in an IC, it is common for multiple power clamps to be distributed in parallel along the power buses.

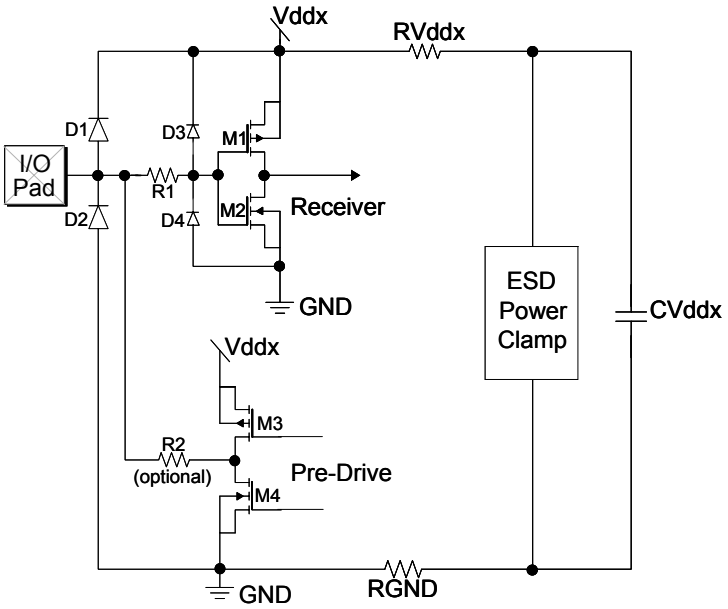


Figure 5: Dual diode I/O ESD protection strategy.

In the ESD strategy of Figure 5, separate secondary ESD protection elements are utilized for the receiver and driver circuitry. During the ESD event described above, a small fraction of the ESD current will flow to Vddx via a secondary path through resistor R1 and diode D3. The benefit of this secondary protection is that any IR drop across R1 will reduce the voltage stress seen across the fragile gates of receiver transistors M1-M2, as compared to the case where R1 is not present. R1 values from 100-5000 ohms are common for protecting receiver circuits. To better protect driver transistors M3-M4, there

is another secondary path to Vddx via resistor R2 and the drain to NWELL parasitic diode of PMOS transistor M3. Note that the use of R2 is shown as an option in Figure 5. This is because many applications such as High Speed Serial (HSS) links or Low Noise Amplifiers (LNA) do not typically permit use of any series resistance between the driver and pad due to performance constraints. Typical R2 values for digital applications can range from 5-100 ohms. This resistance can have a significant impact on the effective CDM robustness of driver transistors M3-M4.

2.2.2 SCR-Based ESD Protection

A schematic of an SCR-based ESD protection strategy is shown in Figure 6 [7-11]. Here the primary ESD protection comprises a diode string triggered SCR clamp from the I/O pad to the GND bus. Therefore, when the I/O pad is grounded during a negative CDM event, most of the positive current will flow from the pad directly to the GND rail via the SCR clamp and then from the GND bus metal grid throughout the IC and package. This direct clamp to GND is an advantage of the SCR-based protection scheme over the prior diode based approach, especially in cases where the GND bus resistance is significantly lower than Vddx bus resistance. In addition, SCRs often have reduced capacitive loading for the same ESD protection level. On the other hand, diode string triggered SCRs can have the disadvantage of higher leakage during normal operation depending upon the maximum operating voltage required.

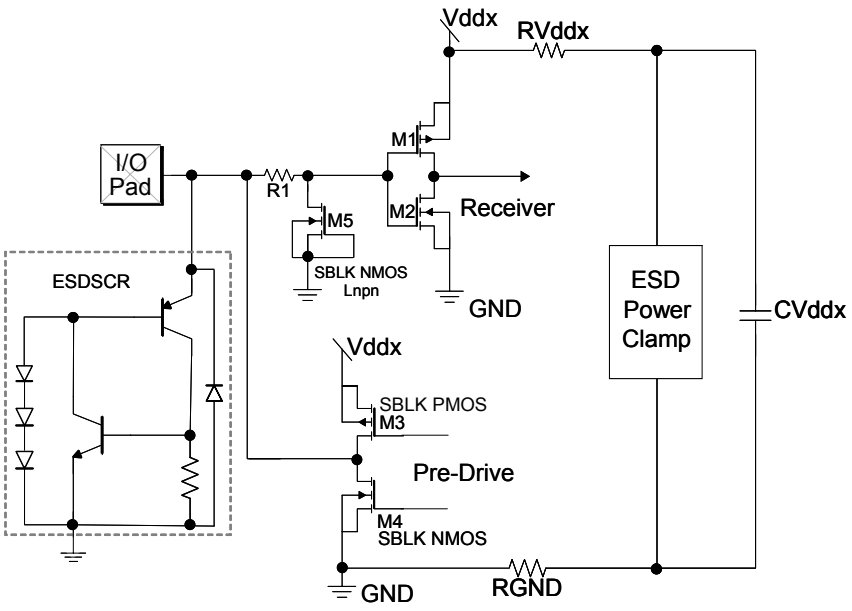


Figure 6: Diode-string-triggered SCR based I/O ESD protection strategy.

Note that, in the ESD strategy of Figure 6, a different type of secondary protection is utilized to protect the receiver transistors M1-M2, as compared to that shown in Figure 5. Here a fraction of the ESD current will flow to GND via a secondary path through resistor R1 and clamp device M5. This clamp is a silicide blocked (SBLK) NMOS transistor which is intended to trigger and conduct as a lateral NPN bipolar during the ESD event. Blocking the silicide in the drain region adds local ballast resistance to the NPN, helping insure uniform current flow across the device width during bipolar

conduction, thereby increasing the failure current (I_{t2}). As before, any IR drop across R1 during ESD will reduce the voltage stress seen across the gates of receiver transistors M1-M2. Note, the secondary ESD NFET is shown for reference only, this example secondary device could be replace by dual diodes, forward biased diode strings or another diode string triggered SCR.

The output drivers M3-M4 in Figures 5 and 6 can also be configured with silicide blocking in the transistor drain regions. Added ballast resistance increases the failure current (I_{t2}) of the drivers in the event they trigger and conduct as lateral bipolar transistors during ESD. In addition, the added IR drop across this silicide block resistance increases the effective drain to source breakdown voltage the transistors can tolerate before suffering permanent physical damage. This provides more voltage margin to driver breakdown for the intended primary ESD path through the SCR clamp. Silicide block ballast resistance is commonly used to harden output driver transistors against ESD, typically increasing Vds breakdown voltages 1-3V, but at a cost in layout area and transistor performance and process cost. Other design options, in place of these that have been discussed here, will also eventually lead to the same limitations.

2.3 Technology Scaling Effects on CDM ESD Robustness

Advancements in process technologies over the past 20 years have brought about impressive reductions in IC cost and gains in performance. Unfortunately these advancements have come at a cost in terms of degraded ESD robustness. Technology scaling has produced smaller and more fragile active devices as well as thinner and more resistive interconnects. For these reasons ESD protection design becomes more challenging with each new technology node [12].

2.3.1 Trends in ESD Robustness for NMOS Transistors

In Figure 7 the robustness of NMOS transistors across multiple advanced CMOS technology nodes is compared. The maximum core Vdd supply voltage is shown as a function of the technology node scaling for both feature size transistor length and gate oxide thickness. Also shown is the simultaneous reduction of the gate oxide breakdown voltage (Vgs) and drain to source breakdown voltage (Vds) under 1.2ns pulse stress conditions. This data was gathered with a Very Fast Transmission Line Pulse (VFTLP) characterization tool which best mimics the true CDM pulse event. All data was gathered on baseline, minimum design rule, fully silicided NMOS transistors. The Vds breakdown data represents the minimum or worst case value measured with varying DC Vgs bias applied during stress.

The data in Figure 7 clearly illustrates the reduction in NMOS transistor CDM robustness with each new technology node. While both the Vgs and Vds breakdown data trend downward with each new technology node, these NMOS devices are clearly more fragile under drain to source stress. It turns out that PMOS transistors (not shown) exhibit similar trends, but are slightly more robust than their NMOS counterparts. Compare, for example, the robustness of NMOS transistors at the 250nm and 45nm technology nodes. A 250nm NMOS receiver device, such as transistor M2 in Figure 5, could survive >12V Vgs stress during CDM ESD, while the 45nm device would fail at only 5.2V. Similarly, a 250nm NMOS driver device, such as transistor M4 in Figure 5, could survive up to 6.3V

Vds stress during CDM ESD, while the 45nm device would fail at only 3.2V. It is clear that transistors become more fragile with each new technology node. This Vds breakdown trend is expected to continue as the channel lengths continue to scale.

It turns out that protecting output drivers with Vds breakdown values of less than 4V is a serious challenge for the CDM ESD designer. This is particularly true in applications which do not permit use of secondary protection or silicide block ballast resistance. Consider, for example, an I/O circuit in a 90nm technology, with ESD protection as described in Figure 5. During a negative CDM stress event the NMOS driver M4 will fail if the local Vds voltage across this device exceeds 3.8V (see Figure 7). Assuming that the peak current produced by the CDM event equals 7.6A, then the ESD elements and interconnect resistances in the primary ESD path must dissipate this current while limiting the total voltage drop seen across the NMOS driver M4 to less than 3.8V. Sizing the ESD elements and interconnects to achieve this 0.5 ohm effective impedance is extremely difficult.

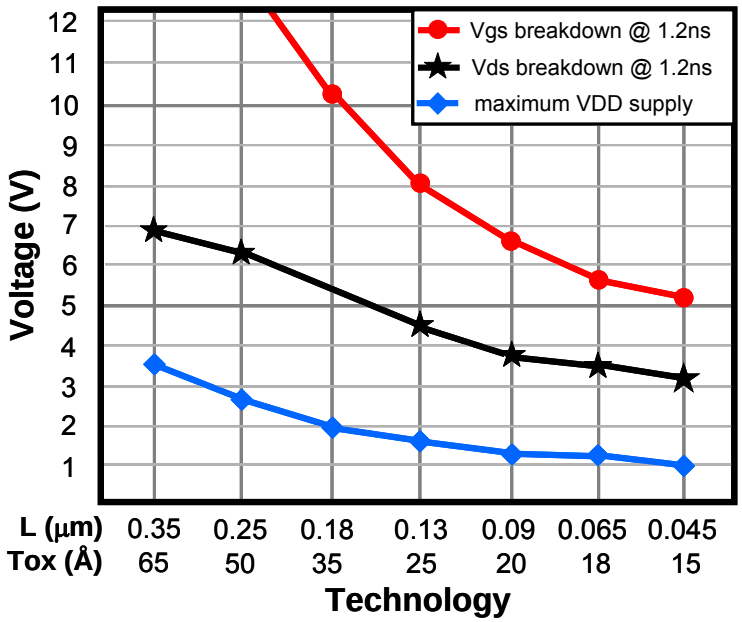


Figure 7: Trends of NMOS transistor breakdown voltages with technology scaling.

2.3.2 Trends in Interconnect ESD Robustness

Another critical technology parameter for CDM design is the maximum allowed current density in the interconnect layers. This trend is shown in Figure 8 typically for a copper metal interconnect. Note that the actual failure current density is dependent on the particular metal thickness but this trend is more of an illustration of the constraint. In the CDM domain the current failure density is actually 3-5 times higher than in the HBM domain. However, if the CDM discharge current level requirements become relatively larger (for example, from large high pin count packaged devices meeting the present target level of 500V) this could turn into the limiting factor for design. For example, at the 65nm node, the current density limit of 0.5A/um requires a 20 um wide bus to carry 10 Amps of CDM current. In addition to the layout area, wider metal interconnect to the

ESD diodes increases the pad capacitance. This in turn may have a negative impact on the circuit speed as will be discussed in Section 2.4.3.

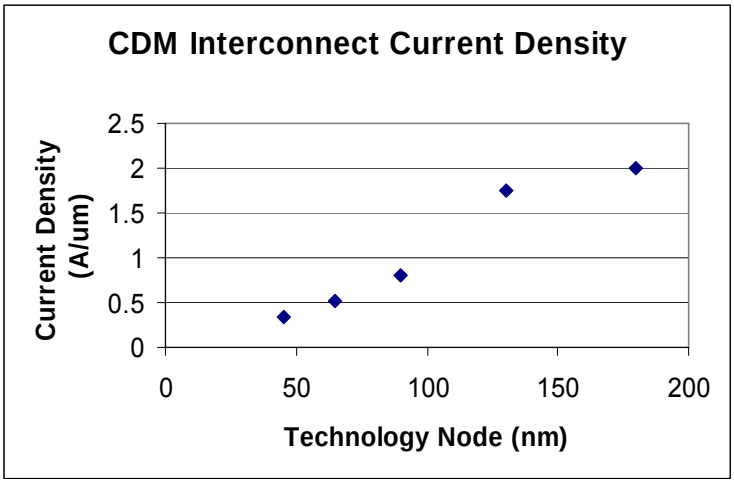


Figure 8: Typical trends for copper interconnect ESD robustness with technology scaling.

2.4 Examples of CDM Impact on Integrated Circuit ESD Design

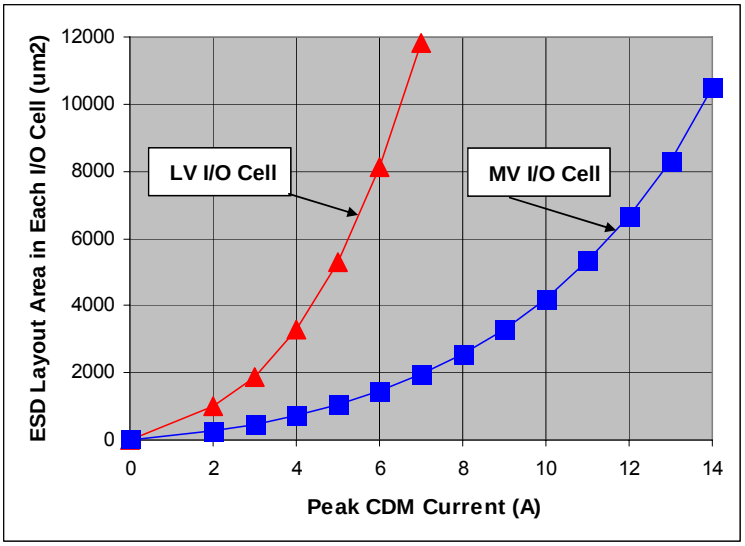
2.4.1 Impact on ESD Layout Area

The ESD layout area on the die required to protect an IC component from a 500V CDM event varies widely with product application and process technology. The target peak CDM current the ESD network must safely dissipate is a primary factor affecting layout area. As illustrated in Figure 4, peak CDM currents at 500V typically range from about 1A, for the smallest die and package sizes, to 16A or greater, for the largest. The process technology, which defines the efficiency of the ESD devices and interconnects along with the fragility of the circuitry to be protected, strongly influences layout area. Finally, applications which do not permit use of added secondary protection or silicide blocking to harden fragile input/output circuits will see significant increases in layout area. In general terms, a very large IC component in the most advanced available process technology with driver/receiver circuits configured in the most fragile manner requires the greatest ESD layout area on the die.

The ESD layout area as a function of target peak CDM current is shown for two example 45nm technology I/O library applications in Figure 9. The two I/O libraries differ in the type of transistor used in the driver and receiver circuitry. The low voltage (LV) I/O library, for use in Vdd=1.1V supply domains, utilizes the core (18A Tox) transistors available in the technology. The medium voltage (MV) I/O library, for use in Vdd=1.8V supply domains, utilizes the I/O (28A Tox) transistors.

The dual-diode and rail clamp ESD protection approach described in Figure 5 was used in both the LV and MV I/O libraries. Small ESD power clamps were distributed in parallel in each I/O cell of an I/O bank within a supply domain. The ESD power clamps in both I/O libraries were built with the more robust I/O transistors. While secondary

protection was utilized to harden the receiver circuitry in both I/O libraries, the application would not allow the option of placing either secondary protection or silicide blocking to harden the output driver devices. Therefore the weak link for ESD in both the LV and MV I/O cells was assumed to be the NMOS output driver M4 in negative mode CDM events, and the PMOS output driver M3 in positive mode events. The measured Vds breakdown values for the NMOS and PMOS driver devices in both the LV and MV I/O libraries are shown in the table in Figure 9. In order to provide a comfortable margin, the ESD networks in both I/O libraries were sized to protect both driver devices to targets 20% lower than their measured breakdown voltages. Therefore, as shown in the table, the target stress limits were set to 2.65V/3.60V for the NMOS/PMOS drivers in the LV I/O library and 3.50V/5.20V for the NMOS/PMOS drivers in the MV I/O library.



		LV (V)	MV (V)
NMOS	**Vds** (meas)	3.3	4.3
	Vds (target)	2.7	3.5
PMOS	**Vds** (meas)	4.3	5.9
	Vds (target)	3.5	4.7

Figure 9: Example estimate of the ESD layout area for I/O cell in two different I/O applications. ESD layout area is plotted versus peak CDM current. The layout area is calculated for two different NMOS and PMOS output driver protection targets.

As shown in Figure 9, the size of the ESD elements in both the LV and MV I/O cells is a sensitive function of the target peak CDM ESD current the ESD network must safely dissipate. The area value includes the area for the ESD diodes and power clamp in each I/O cell. Note that, for both curves, the ESD layout area increases exponentially with peak CDM current. In fact, for the LV I/O cell, the increasing slope of the curve suggests that CDM current targets above about 7A are not realistic since, beyond this ESD current ceiling, huge increases in layout area are required to a achieve a small incremental increase in CDM current. It is important to note that the exponential nature of the ESD layout area vs. CDM current target curve is common to all process technologies and to all ESD protection schemes. However the actual ESD current ceiling will vary considerably from product to product, depending on process technology, circuit application, and ESD protection scheme.

It is obvious from the drastic differences between the two curves in Figure 9 that the Vds protection target for the output drivers M3-M4 has a major impact on the ESD layout area required at a given CDM current. While 7A CDM protection can be achieved for the

MV I/O cell with about 2000um^2 of ESD layout area, the LV I/O cell requires almost 12,000um^2 to meet the same protection level. This is a 6X increase. It should be pointed out that the layout area for full I/O cells (excluding ESD) in advanced CMOS technology products typically ranges from 2000um^2 to 8000um^2. Therefore, depending on the CDM current target and the I/O application, the ESD layout area may grow to dominate the overall I/O cell layout area. This is an issue of particular concern for IC components in large packages.

2.4.2 Impact of the ESD Design Window on CDM

It has been well established through various studies that the "ESD Design Window" is rapidly shrinking with advancement of silicon scaling technologies [10]. As shown in Figure 10, the window is essentially defined as the space between the IC operating voltage (Vop) and the IC breakdown voltage (Vbd). Although the operating voltages have been slowly reducing (flattened out in the 0.9-1.2V range), the breakdown voltages have been degrading at a much faster rate giving rise to the reduction in the window. The limitation of the breakdown voltage could come from either oxide breakdown voltage under ESD conditions (for input buffers) and/or from the thermal junction breakdown voltage (for output buffers). This is indicated as the "IC Reliability Constraints" in Figure 10. On the other hand, for scaled technologies the metal interconnects are getting thinner, leading to more resistive busses for ESD design applications. Thus designing to a given ESD current level the voltages at the I/O pads build up to the critical breakdown values at even lower current levels. This metal restriction is shown as "Thermal Failure" in Figure 10. This design window reduction applies to any type of IO protection strategy even though some advanced designs might give a slight advantage. Nevertheless, the overall reduction makes it difficult to design for any high HBM or CDM levels. This is further elaborated in Figure 11.

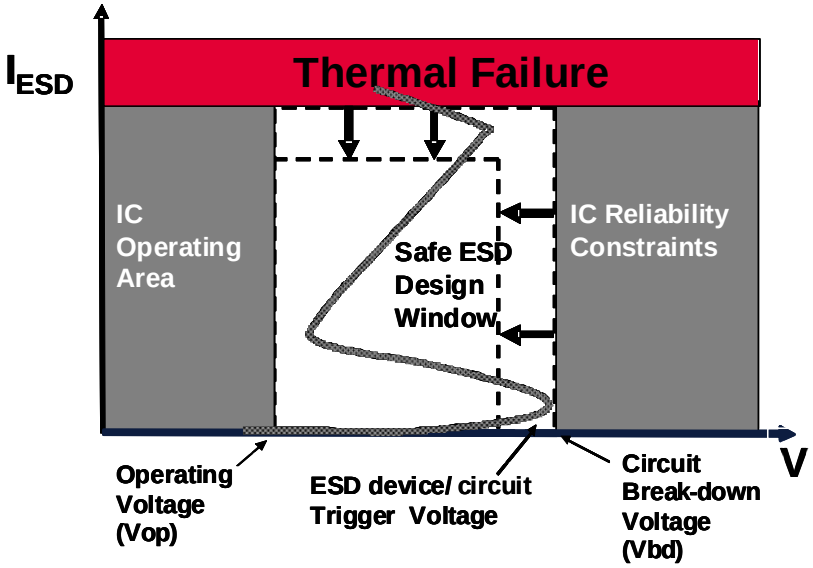


Figure 10: ESD Design Window Definition

Figure 11 shows how the ESD design window (Vbd-Vop defined in Figure 10) has scaled going from 350nm down to 45nm technology nodes. The design window has shrunk by approximately 2.7X scaling from 350nm down to 45nm while the ESD targets have remained constant. The ESD design window reduction requires either larger ESD devices

to clamp the voltage to lower levels or it requires significant innovation in ESD devices as technologies scale. Increasing the ESD device sizes to compensate for the design window scaling is not practical for two main reasons: 1) the area allocations for ESD devices/circuits are scaling down at each technology node, and 2) the capacitive loading requirements are simultaneously also being reduced for each new technology generation.

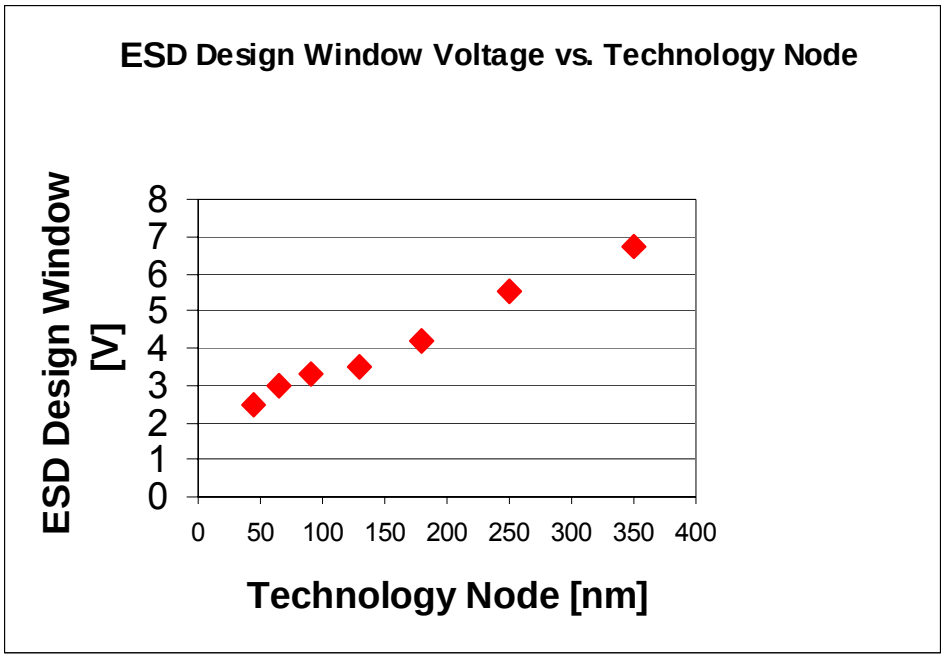


Figure 11: The ESD Design Window versus Technology Node. (In terms of difference between maximum operational voltage and oxide breakdown voltage)

2.4.3 Impact on HSS, RF and Analog Applications

In Figures 12 and 13 the allowed ESD capacitive loading is shown on the x-axis and on the left y-axis the High Speed Serial (HSS) link data rate is shown and on the right y-axis the CDM maximum current supported is shown. For the allowed ESD capacitive loading for this example it assumes there is a 50% cancellation of the ESD capacitance occurring through known techniques such as Tcoils for example. The net allowed ESD capacitive loading will actually end up being approximately 50% of the values shown in Figures 12 and 13. The peak CDM current supported in 65nm and 45nm is shown in Figures 12 and 13 for double diode based ESD protection and for forward biased SCR based ESD protection, respectively. One of the key items to notice for the HSS data rates is how the capacitive loading requirements going from 3-4 gigabits/sec to 10-12 gigabits/sec make it necessary to reduce the capacitive loading of ESD protection circuits by approximately 3X. In HSS circuits and LNA circuits, resistances and secondary protection are typically not allowed as described in previous sections thus the data from simulations shown in Figures 12 and 13 assumes no secondary protection. The CDM current is shown for positive current at the I/O pad, which results in the silicon substrate being charged up negatively; often representing the worst case CDM condition.

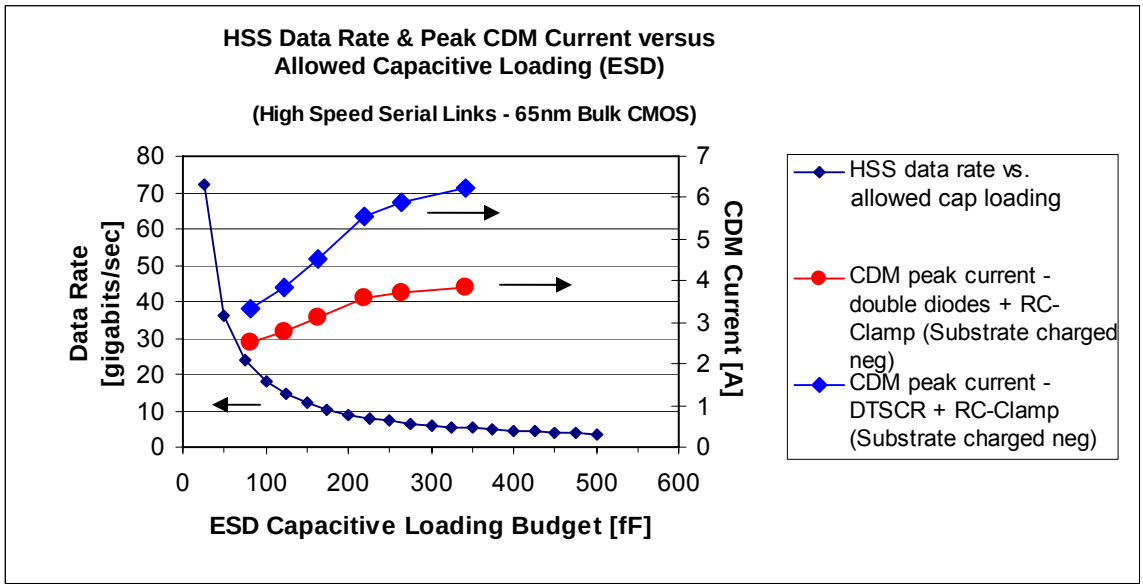


Figure 12: Data Rates and Peak CDM current design capability vs. Allowed ESD Capacitive Loading Budget for two different design approaches in 65nm technology node

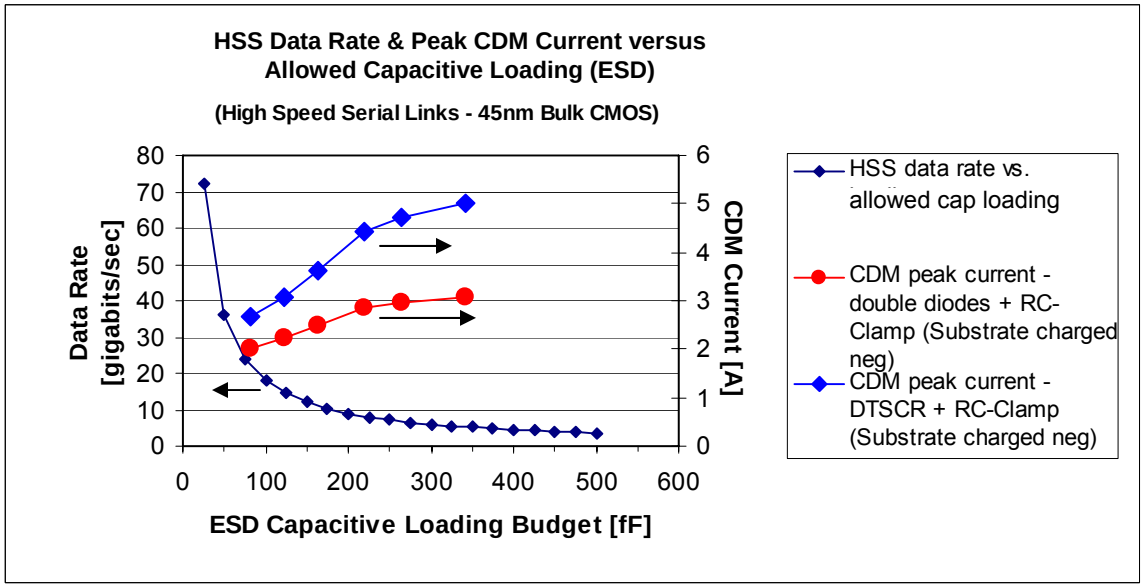


Figure 13: Data Rates and Peak CDM current design capability vs. Allowed ESD Capacitive Loading Budget for two different design approaches in 45nm technology node

RF high speed designs are even more restrictive than standard high speed SERDES designs. For RF pins with 5-10 GHz performance requirements ESD design can be quite a burden. The Low Noise Amplifier (LNA) input circuits are especially intolerant to ESD protection device capacitance. In these circuits the ESD ground is often isolated from the LNA ground and separated by diodes as shown in Figure 14. With the usual requirement of less than 100 fF capacitance for the ESD diodes it is difficult to achieve even 1kV HBM protection without damaging the gate oxide. This is mostly due to the on-resistance

of the small protection diodes used to meet the circuit RF functional requirements. CDM performance can be even more challenging than HBM or MM for these RF applications.

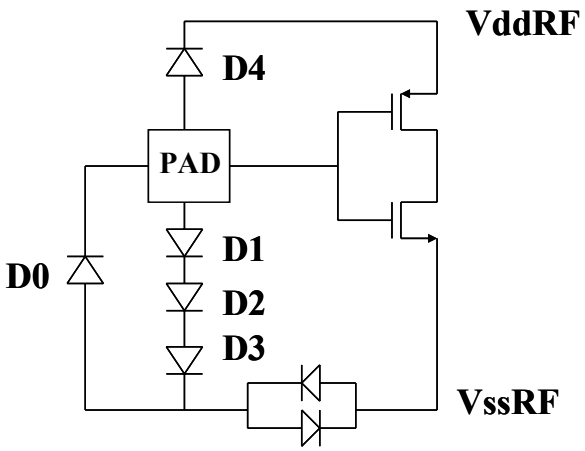


Figure 14: Typical Low Noise Amplifier (LNA) pin with diode protection.

The reasons for the low CDM performance are: 1) absence of secondary clamp, 2) smaller sized protection diodes that build up the voltage to critical levels even for small CDM currents, and 3) isolation of the ESD clamp ground from the RF buffer ground. Regarding restriction #2 the situation could become worse if the input pad is directly connected to the core gate oxide in order to achieve high speed input performance. The clamp diodes must be smaller in size to meet the low total capacitance budget at the pin.

RF pin application chips with system on chip (SoC) function usually employ small BGA packages of 8mm X 8mm or 10mm X 10mm. The peak currents are quite low, not more than 3-4 A at 500V. However, these sensitive RF designs with small clamps can often only be effective for CDM current levels of 2 A or less, thus severely limiting their CDM performance to 200-300V. For example, as shown in Figure 13 for an RF application chip with 10mm X 10mm package size the LNA input ESD design can only handle 2A which corresponds to only a passing level of about 200V.

2.5 Package Effects and Package Trends

Advances in Packaging technology are based on requirements of the different market segments [13]. For computer applications, advances are based on performance. While for the consumer market it is price and robustness. For automotive and military applications it could be temperature sensitivity and reliability. Each type of package is then designed and selected according to the application. This proliferation has gone from the standard Dual-in-Line (DIP) packages to Multi-chip Modules (MCM) and to Flip-chips and Stacked Die or even Stacked Packages. Eventually we could come to Wafer Scale Packages or (WSP).

Although not particularly considered in the past or even at present, during the package development some attention should also be given to the ESD effects as well. The

aggressive technological advances into newer type of packages might very well determine the achievable ESD performance for overall adequate reliability.

The most serious impact that packages have is on CDM where its performance strongly depends on the package type and package lead design. If the qualitatively assessed CDM risk is now imposed the TQFP package might pose lower CDM performance while the micro-star BGA (u*BGA) can show relatively better CDM performance. This is simply related to the peak current that is discharged during the stress and directly depends on the effective package capacitance. Some of the most significant impacts of packages on CDM would come from a variety of packaging factors. What could influence the CDM peak current and hence the CDM performance is summarized for a BGA package below:

- The die size where larger die would mean more capacitance
- The mold compound material and its thickness
- The lead frame metal routing including the number of pins

Chips with larger die sizes that incorporate larger packages would naturally pose a larger threat to CDM design. For example, the measured peak current at 500V as a function of package area is shown in Figure 15 [14]. Note that while the HBM current at 2kV is independent of the package size the CDM current rapidly increases with package area.

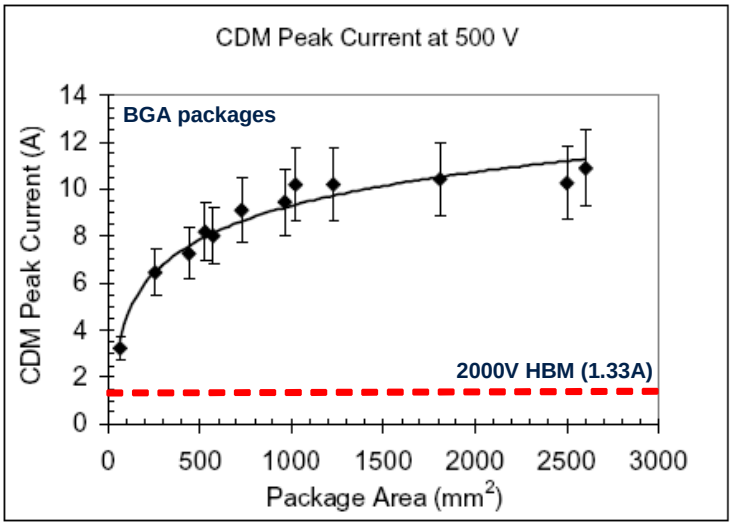


Figure 15: CDM Peak Current data for BGA packages at 500V CDM.

The most critical design constraint for CDM comes from the trend towards higher pin count packages. This market is driven mostly by ICs for internet switching (with high bandwidth) and microprocessors where very high pin count packages are commonly used. This bandwidth can be achieved by incorporating a balance between high speed IO's and wide parallel busses. Designs for such markets use chip to chip interfaces with DDR2 (250MHz), RLDRAM (500MHz), and SERDES (6GHz). Although the trend for increased off chip speed may reduce the number of IO's required, it also leads to higher number of power pins for thermal performance. The net result is an increase in average pin count. This continued trend for high pin count is depicted in Figure 16 for BGA packages.

Around the 32nm technology node the pin count is expected to reach the 3000 level. At this pin count the package area would exceed 2000 mm^2. Indeed both the die area and the package area would contribute to increased CDM peak current at a given voltage stress level. So invariably designs requiring high speed IO's tend to be placed in IC packages with high pin count which consequently places a constraint on the CDM design capability.

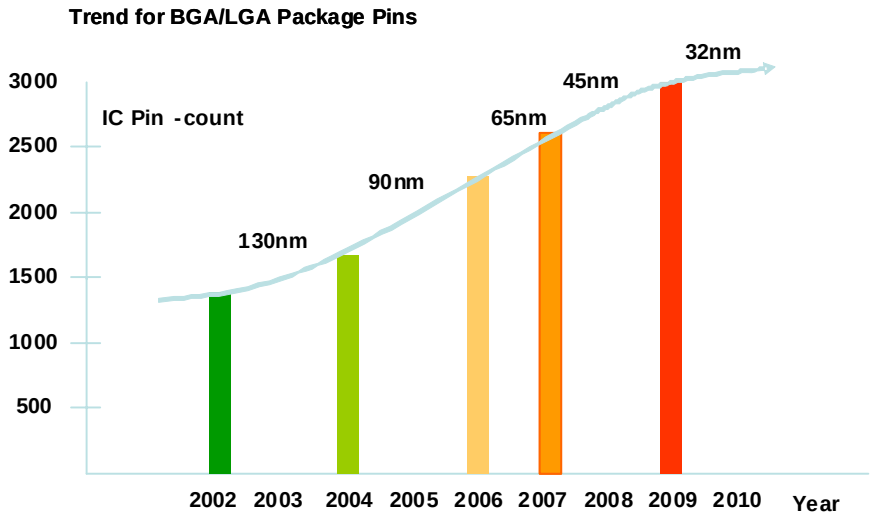


Figure 16: Trend for high pin count BGA Packages

Meeting a 500V CDM level for larger packages will in general not be possible. The more realistic design windows for CDM for package sizes exceeding 1000 mm^2 are shown in Figure 17. First, it is seen the CDM peak current increases as the package area increases (assuming the same thickness package) and that this behavior linearly moves to higher current levels at higher stress levels. For example, a 1000 mm^2 BGA would produce 4 Amps at 200V stress and more than 10A at 500V stress. However, the practical design windows dictated by circuit performance would limit the achievable CDM level. Based on the data rate simulations shown in Figure 12, for the 65nm HSS IO designs with speeds of 5-20 Gb/s the peak current in ESD design is restricted to between 2.5A to 6A. This is shown by the blue box in Figure 17. At the 45nm node this would degrade to 2A to 5A range, further lowering the achievable CDM levels. Figure 17 clearly illustrates that for these HSS designs with large package areas the CDM performance is limited to between 200V and 300V.

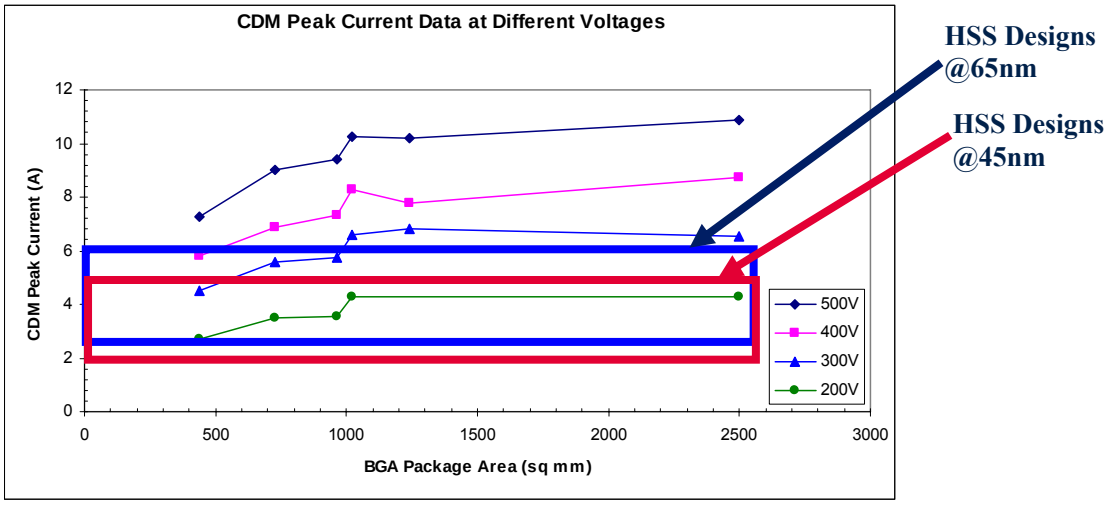


Figure 17: CDM Peak Current data for various packages at various CDM stress levels.

In this manner we can see that as chip sizes are made larger and built in complex packages with many more pins (>2000) the CDM stress current will continue to increase in magnitude. Combined with the package effects presented here, RF designs that can tolerate very little capacitance from the protection device will have difficulty meeting the ever larger CDM currents. In the future, CDM package issues will become worse for stacked packages and multi-chip modules. Moreover, conversion to new organic materials for environmental safety could potentially exacerbate the situation. Therefore, package engineers and ESD engineers need to work in close collaboration to maintain package performance and ESD reliability!

2.6 ESD Designer's Perspective on Realistic CDM Targets

The overall expected performance for CDM while meeting all of the design constraints is already challenging today and in the future will become even more of a challenge. In order to understand this we need to examine the total picture of the IC packages ranging from small pin count (<100) to medium pin count (300-500) and high pin count (500 to >1000) ranges. This package map is illustrated in Figure 18. The top row shows the package type trends as they progressed from DIP to BGA to LGA. Eventually all packages will converge to become BGAs. The second row shows the corresponding number of pins. Based on physical data the markers for the package areas corresponding to the package pin numbers are shown in the third row. After measuring actual peak currents at various stress levels for the different area (pin count) packages the estimated CDM performance chart for different IO designs is shown. This data was generated by measuring the CDM discharge currents from various sized packages with designs constraints defined in terms of maximum tolerable current levels in each case. For example, if a practical IO design with its CDM protection design can handle 8A of peak current, for pin counts up to 1000 the currently accepted CDM level of 500V can be met. But if the pin count goes beyond 1000 to nearly 2000, the CDM performance can only be about 400V. These numbers currently reflect 45nm and 65nm technologies. The next row for high speed IO designs shows that packages devices with >200 pins or a package area

of >250 mm^2 cannot meet the same expected 500V. It should be noted here that beyond 2500 pin packages the performance data is only an extrapolation based on known relation between package area (capacitance) and the CDM peak current as a function of stress voltage.

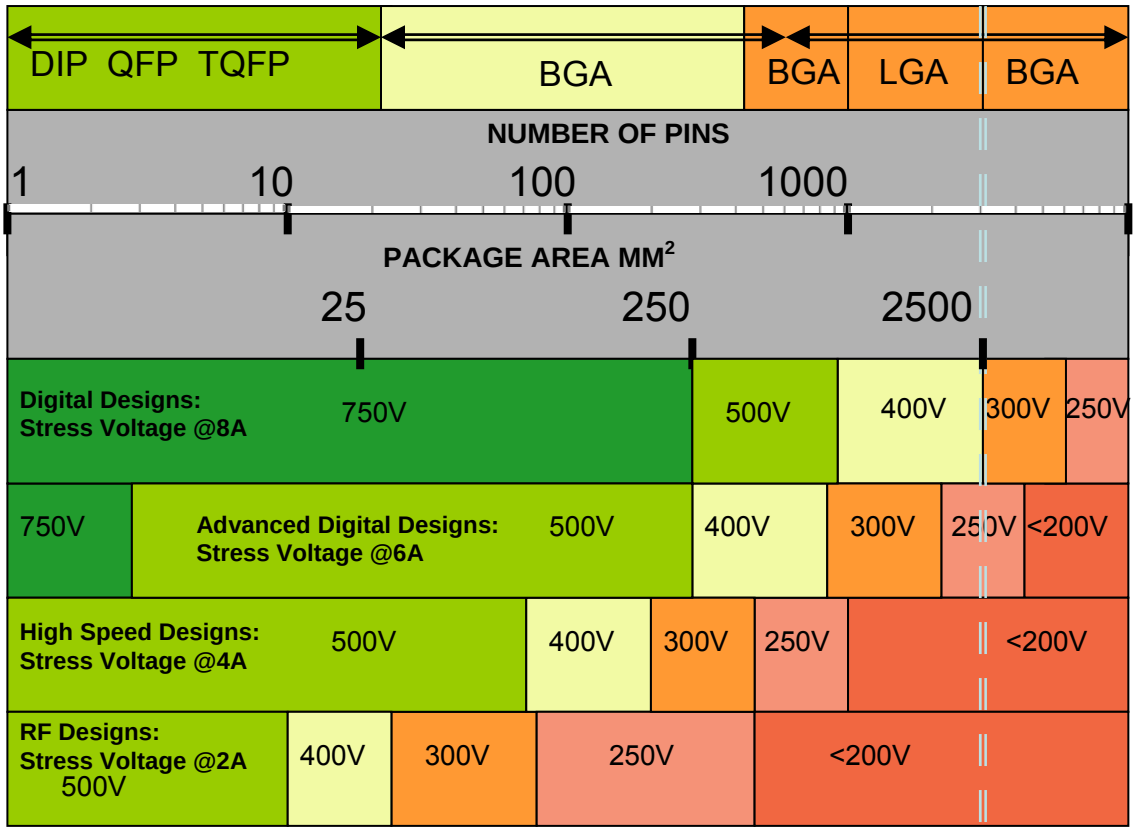


Figure 18: CDM package map for 65nm and 45nm designs. Products with >1000 pins or 1200 mm^2 area are limited to 400V CDM passing voltage for all practical designs; this would reduce to 300V for high speed Serdes designs. The vertical dashed line represents the state-of-the art in high pin count packages.

Following this trend, the CDM performance restriction faced by RF designs is indicated in the last row of Figure 18. Since most of the RF designs tend to be in smaller IC packages they are not expected to face the severe degradation of performance as the High Speed Serial Link (HSSL) IO's. However, even at smaller package areas the RF pins are sensitive for CDM design as noted in Section 2.4.3 and thus are challenged to meet 250V level for packages with even 300 pins.

2.7 Further Technology Scaling Effects and Additional Impact to Realistic CDM Targets

As we move towards 22nm technologies and beyond even this 250V level is certainly bound to place more severe restrictions on CDM protection design due to the impending further scaling effects and the drive towards higher circuit speed performance at data rates reaching 40 Gb/sec or more. A revised package CDM map for the 22nm node is projected in Figure 19.

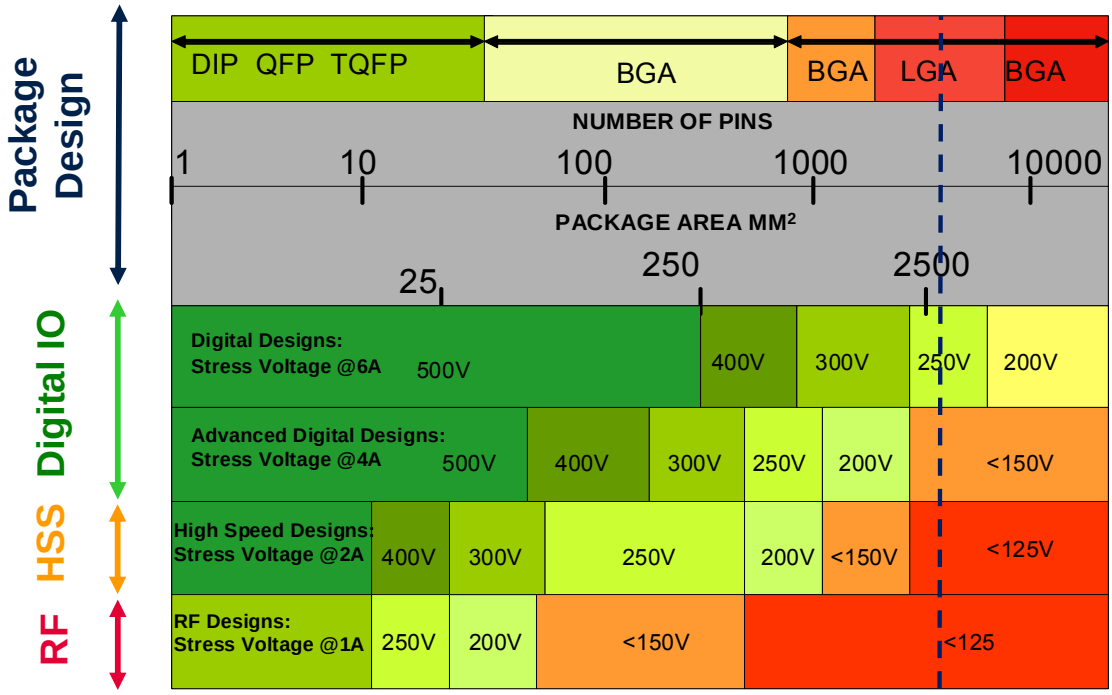


Figure 19: CDM package map projected for 22nm designs. Products with >1000 pins or 1200 mm^2 area would be limited to <150V CDM passing voltage for all HSS and RF designs.

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Chapter 3: CDM Related ESD Control in Assembly Lines

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Ron Gibson, Celestica
John Kinnear, IBM

The trend regarding the ESD robustness of semiconductor devices according to the Human Body Model (HBM) and the Machine Model (MM) is pointing to lower and lower values [1]. There is a general concern by many companies that they cannot handle these sensitive devices. However, if ESD-protective measures in the assembly lines are set up according to international standards such as ANSI/ESD S20.20 [2] or IEC 61340-5-1 [3], these devices can be handled without any adverse effects from HBM and MM ESD (see also [4]). The 2007 editions of both standards are more or less aligned and provide rules for the safe handling of "electrical or electronic parts, assemblies and equipment susceptible to damage by electrostatic discharges greater than or equal to 100 volts Human Body Model" (taken from ANSI S20.20).

Therefore we do not have to expect ESD failures, related to the Human Body and Machine Models, if an ESD program is implemented that follows one of the above referenced international standards. However, HBM / MM like hazards are only two of the risks that can be found on an assembly line. It is also necessary to prevent the charging and subsequent hard grounding of ESD sensitive devices or printed circuit boards (PCB) which results in a charged device model ESD event. The ESD Association's Technology Roadmap for Semiconductors also provides a trend chart for CDM robustness.

What do international standards require to avoid CDM like ESD hazards? Many of the basic ESD protection measures for HBM protection also protect against CDM related problems, although it would not be called special CDM protection measures. Examples for these are wrist straps or table mats. If an operator is not grounded he could induce charge on a device or PCB without directly damaging by a discharge. But when the device or PCB is placed on a metal surface, it could be damaged by a CDM like discharge. On the other side a grounded dissipative table mat avoids dangerous potential differences between various items in the production area, and also avoids the hard discharge of a charged device. It is therefore a CDM protection measure. Many examples like these can be found. The situation is summarized in Figure 20, which shows that basic CDM protection is already part of the basic ESD protection process that is in place in the majority of EPAs world wide.

As an add-on for CDM specific protection, international standards require the removal of non-essential insulators that can become highly charged and require a strategy on how to handle process relevant insulators.

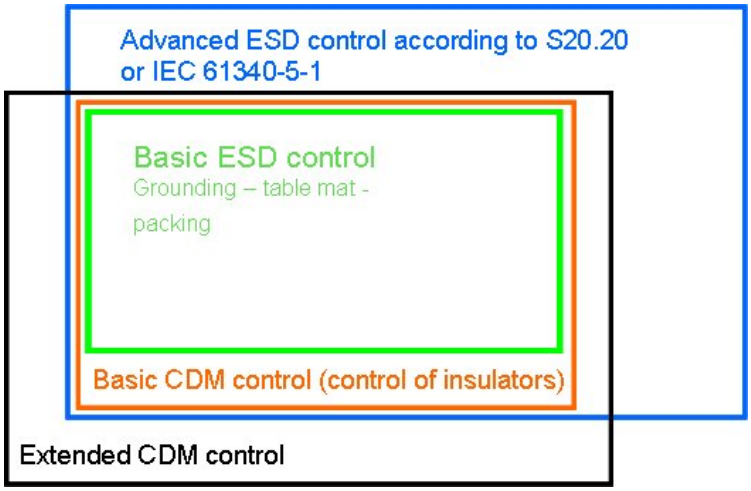

Figure 20: Relationship between General ESD Control and CDM Specific Control

3.1 Basic Idea of CDM Protection

Many assembly processes cause charging to take place. However, the charging alone is not critical and can also not always be avoided. Therefore, a detailed analysis of possibly damaging hard discharges of a charged device/board has to be performed for every single process step.

Basically there are several ways to analyze the CDM-like risk. Some approaches are already published ([5-7]) to give the end-user a guideline in analyzing the CDM-like risk or the process capability of the respective production line. The basic idea of these approaches is shown in Figure 21.

The respective measurements will then answer the three main questions:

1. What is the process capable of protecting in relation to CDM?
   Note: Even if the values for CDM robustness determined during device level testing are not directly comparable, we know by experience that we normally have no automated handling problem in a controlled line when the measured charging values do not exceed the CDM robustness values.

2. Where are the ESD problem areas in the process, and what risk do they pose to CDM sensitive devices?
3. How effective can any changes to the process be for controlling CDM risks of sensitive items?

The following sections give examples of how a process can be analyzed to avoid CDM like failures.

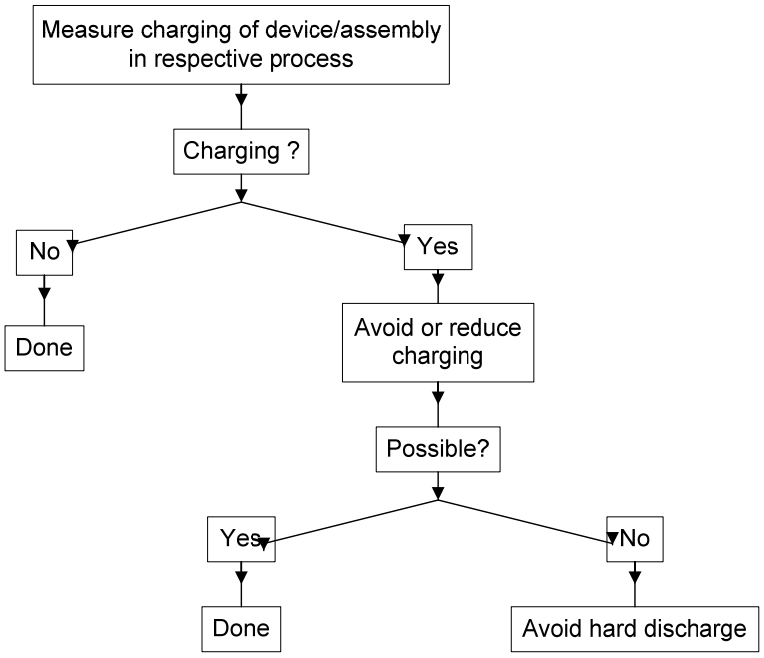

Figure 21: CDM risk analysis flow

3.2 Process Related Risk Analysis

While doing the investigation of device and PCB charging it also has to be taken into account whether or not these charging values are dangerous for the object; i.e. it has to be analyzed whether the charged object "sees" a contact to ground (or another conductive object at a different potential), which is introducing a dangerous hard discharge (CDM like event) to the charged object. If that's not the case, the charging will normally not cause any damage to the object (electrostatic problems like attraction of particles by charged objects will not be discussed here).

This results in an analysis of every single process step by asking the following questions:

- Is there charging of the object being manufactured?
- Is there a chance for a hard discharge in this or the next process step?

If there is no charging, there is no possibility for a hard discharge. If there is no hard discharge, there is normally no possibility of CDM damage.

3.2.1 Theoretical approach

This will be explained in some simple examples that can happen in a typical PCB assembly line:

1) An uncharged PCB is transported on a conveyor belt from process step A to process step B in a closed tunnel. In order to be able to look into the tunnel the cover is made of a transparent material. To keep costs low the cover is made of insulative, highly chargeable Plexiglas. While the (initially neutral) PCB is running underneath the highly charged Plexiglas the electrostatic field of the Plexiglas results in a charge separation on the conductors of the PCB. This is not damaging to the PCB! If the PCB exits out of the charged transport tunnel without having seen a metallic contact (or an arc to a nearby piece of metal) the charge recombines and a neutral undamaged PCB arrives at the next process step.

Note: The use of a grounded, dissipative cover prevents the charging of the cover and therefore avoids the field-induced charge separation on the PCB. This makes the risk analysis much easier but is not absolutely necessary.

2) The same uncharged PCB now comes to a process step, where it is left in a charged state. A possible example is when a charged barcode label is attached to the PCB, or when the PCB is held in place by a bar or stop at the end of a conveyor while the conveyor belt continues to run and charges up the PCB by rubbing. Such processes can charge the PCB to several hundred Volts. If the metal parts of the PCB (e.g. connectors or metal lines) are not contacted by (or are not coming close to a grounded conductive object), there is no risk for a hard discharge (or arc) and the process step can be quoted "safe" independent of the charging. Additionally it is necessary to determine what happens to the PCB in follow-on process steps. If the PCB comes to a process step where it discharges slowly and in a controlled way (e.g. by the temperature at reflow soldering or by the relative humidity while storing in a magazine) no further measures are necessary. If the charged PCB is going directly to a process where it contacts another conductor (e.g. at testing), the charges must be drained off before the first contact happens (e.g. by using ionization).

3) The same uncharged PCB now comes to a process step, where it is charged during the process and contacted immediately afterwards, i.e. a hard discharge can happen immediately after the charging event. In this case there is definitely a risk for a CDM like ESD event. A typical example for this is the In-Circuit-Test (ICT). The PCB is pressed down by plastic pins made very often of highly chargeable material. This charging is transferred to the PCB by induction. During the electrical measurement the PCB is contacted with metallic Pogo-Pins and a hard discharge from the PCB into the tester can occur.
Note: Very critical during such "closed" process steps is the fact that the problem can be overlooked very easily since the PCB is not charged before and after the process but can nevertheless be damaged during the process.

Table III shows possible ESD risks during different process steps in a typical assembly line for PCBs or control units. It also gives an overview of the risk during standard process steps and shows additionally how to perform a process related risk analysis.

An example of how Table III is to be used is explained using the process step "placement of ESDS" onto the PCB (ESDS = ESD sensitive device). Two different ESD risks can occur:

i) The PCB can get charged during the process step before and discharges into the ESDS.
ii) The ESDS gets charged because an ungrounded or insulative pick-up tool (suction cup) is used for picking and placing and the charged ESDS discharges into the PCB. This can especially be risky if a lot of other components are already placed onto the PCB (bigger capacitance).

In both cases the charging voltage should be measured using an electrostatic voltmeter.
For case i) The PCB should be measured to determine whether the board, especially whether the metal lines on the boards are charged. If the charging voltage is too high it should be reduced, e.g. by using an ionizer.

For case ii) it would be best to measure the charging of the device while it is hanging on the suction cup. If that's not possible during assembly the charging of the bare suction cup in a "park" position can be measured and the charging of a device needs to be derived from this measurement. If that's also not possible at least the resistance to ground of the suction cup should be measured.
If the charging voltage is too high, the use of a dissipative and grounded suction cup may improve the situation. Additionally an ionizer might be necessary.

For the rest of the process steps described in Table III (and of course also for those not described there) the CDM related ESD risk analysis always has to be performed in the same way:

- Check whether there is a high charging of the devices or the PCB
- Check whether there is a risk for a hard discharge of the charged device or PCB

It is the best to do such a process related risk analysis together with the respective process engineer since he should be able to explain how the process is really running and he should also be able to run the process in a single step mode (if necessary). This allows doing all the necessary measurements in a "real life" situation.

Table III: Possible ESD risk in typical PCB assembly process steps

Process Step	Possible Risk	Test Method	Remedy
Placement of non ESDS (e.g. resistor, capacitor,…)	The board can get charged during placement, since a lot of non ESDS are sent in highly chargeable packing materials	Measure the charging of the board using an electrostatic voltmeter	Install an ionizer after placement of the non ESDS
Placement of ESDS (Discretes and ICs)	i) The board is charged due to the process steps before and discharges into the ESDS	Measure the charging of the board using an electrostatic voltmeter	Install an ionizer before placement of the ESDS (application specific limit)
	ii) The ESDS gets charged due to the use of ungrounded or insulative suction cups at pick and place and discharges into the board	a) Measure the charging of the IC while it is hanging on the suction cup b) Measure the charging of the suction cup c) Measure the resistance to ground of the suction cup	Use conductive/dissipative suction cups, that are grounded; if necessary, use an ionizer to reduce the charging
Reflow soldering	No risk, if there is no metallic contact to pins; charging is decreased due to higher temperature		
In-Circuit-Test (ICT)	Downholder pins and/or (transparent) cover of the ICT are often made of highly chargeable materials; especially the downholder pins can be very close to the sensitive pins of the ESDS and induce charges on the ESDS; during the contact of the pogo pins from underneath a hard discharge can occur (CDM like event)	Measure the charging of the board using an electrostatic voltmeter	Use dissipative materials for downholder pins and/or plastic cover and ground them. Use 2stage pogo-pins.
Final testing	Depending on the way the testing is performed, a charging of the board can happen followed by a hard discharge into the tester	Measure the charging of the board using an electrostatic voltmeter	Avoid the charging by using ionizers or other appropriate measures (depending on the actual process)
Rework stations	Normal ESD risk by operators or by ungrounded tools (including soldering iron). Device storage boxes often made of non-dissipative material.	Measure the charging of the board/operator using an electrostatic voltmeter	Use ESD protective materials and ground them (incl. soldering tip (limit < 1MOhm))
Internal transport and packing (especially after final test)	Risk of charging by the use of non-dissipative packing materials. Normal handling risk during packing.	Check packing materials (measure charging or resistance). Check handling procedure	

3.2.2 Field examples

Recent experience has shown that real CDM failures (i.e. failures created by a hard discharge of the device with resulting failure modes similar to those found during qualification testing) happen mainly during semiconductor manufacturing and testing. However, CDM and CDM-like failures happen outside semiconductor manufacturing processes as well. For example, CDM failures can happen in printed circuit board (PCB) assembly operations. Failures due to so-called charged board events can occur when a complete PCB (or part of it) is charged and subsequently discharged. CDM-like failures may result in a different, more intense, failure mode. However, situations of CDM-like failures can be related to CDM events and the techniques used to control either failure type within any manufacturing or handling process are the same.

Four examples of CDM and CDM-like failures have been included in the following sections.

CDM failure during automated semiconductor testing

Figure 22 shows the failure rate trend of a device in a BGA-293 package. The device had a CDM robustness of 250V and analysis indicated that the failing devices had a CDM-like failure signature. The device shows a high percentage fallout in the ramp-up phase for this new product at the IC supplier's test site. Upon analysis, the failure signature of these devices was the same as those found on failed devices during CDM qualification testing. The root cause of the failure was the high charging of the device during testing (up to 1000V), induced by an insulative nest which supports the mould compound on the backside of the device. The problem was discovered in an assessment of the handling process and the problem was solved by minor but effective improvement in the test handling (dissipative support materials) which restored the safe manufacturing instantaneously. It was not necessary to redesign the device. It was manufactured and shipped without any further problems in manufacturing or in the field.

Occasional problems during the ramp-up phase due to specific handling steps have been encountered for devices having a wide range of CDM robustness (even above 1000V).

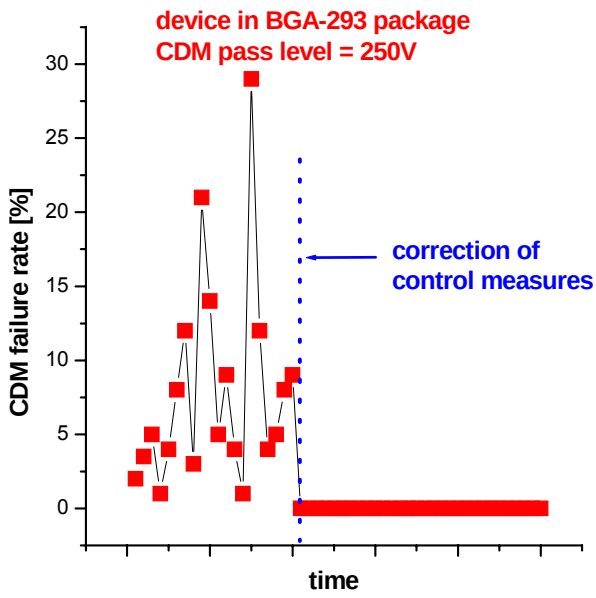

Figure 22: CDM-type failures occasionally occur during ramp-up of new products. After correcting the CDM control measures a safe manufacturing was regained and no further problems appeared.

CDM like failure during manual semiconductor testing

In a semiconductor backend fails of an ESD sensitive device in ceramic PGA package occurred. The "normal" ESD protective measures like operator grounding have been installed and controlled on a regular basis. After a detailed analysis of all process steps [8] the testing process was determined to be the root cause for the fails. During the manual loading/unloading of the device for testing the ZIF-socket had to be opened and closed very often. By doing this, plastic parts of the sockets rubbed against each other and charged the socket to more than 1000V. This was transferred to the device by induction resulting in a charge separation inside the device. When the socket was closed completely (by closing the lever), the (charged) pins of the device were pressed into the contact springs of the tester which resulted in a hard discharge.

Note. The problem could be solved by using an antistatic spray at the beginning of each shift, which reduced the charging dramatically.

CBE failure in an assembly line for automotive control units

A device with a CDM robustness of > 500V, which was used in the control unit of an air conditioning system of a car, showed CDM-like fails during assembly of the PCB, after assembly into the car (0 km) and in the field (at the end user). In all cases the gate oxide of a transistor was damaged.

The normal ESD protective measures - like grounding of operators or tables, internal transport boxes etc. – haven't been perfect, but this could not explain the observed systematic failure. A process related risk analysis, performed using Table III, did not lead to findings during the first assembly steps like placement, soldering, or ICT. For the second test step the metallic fixture, which holds 10 PCBs, had to be lifted in an isolated way for the measurement. By performing charging voltage measurements using an

electrostatic voltmeter it could be shown that the fixture and with it all 10 PCBs that have been metallically connected via the heat sinks to the fixture were charged to several hundred volts. For the electrical testing the PCB was contacted with the (metallic) pogo pin of the tester directly at the gate of the transistor resulting in hard discharge of all 10 PCBs. Depending on the charging voltage and the respective discharge current the failure could be detected immediately, at 0 km, or – worst case – only later in the field.

In the course of the analysis of this process step a corrective action could be defined together with the respective process engineer, which did not disturb the performance of the process. The fixture was grounded via 10MΩ resistance, which was sufficiently high to 'isolate' during testing, but low enough to avoid the charging of the fixture during lifting.
Detailed analysis was required in this case, because the PCB was electrically neutral before and after the process step of electrical testing.

CBE failure in a mobile phone production line
A mixed-signal device was used on a PCB for a mobile phone and showed a high failure rate during production. The "normal" ESD protective measures like operator grounding, grounding of work surfaces and the use of ESD protective packing were analyzed and improved but these measures did not solve the problem. A process related risk analysis was performed to find the root cause of the failures. It was sufficient to check the process steps from placement of the IC to the first measurement where the damage was detected. After excluding the processes of placement, reflow soldering, and the testing itself, the failure must have happened between reflow soldering and testing. The only process steps in between were the placement of a barcode label onto the finished PCB and pressing the PCB out the metallic fixture (used for mechanically fixing the PCBs for placement).

The analysis of possible charging and discharging events showed that the PCB was charged to several hundred volts during the automatic placement of the insulative barcode label. The charging was definitely not the root cause for the damage (proved by electrical re-tests directly after charging and softly discharging). However, when the PCB was pressed out of the fixture with grounded metallic needles, the needles contacted printed leads on the PCB, which were directly connected to the damaged pins of the mixed-signal device (see Figure 23).

The contact resulted in a hard discharge which damaged the device. This was experimentally verified in the assembly line by charging (applying several charged barcode labels), discharging and immediate electrical re-test.
Note: It would not have been possible to find the root cause of the failure without implementing the "normal" ESD protective measures before doing the process related risk analysis.

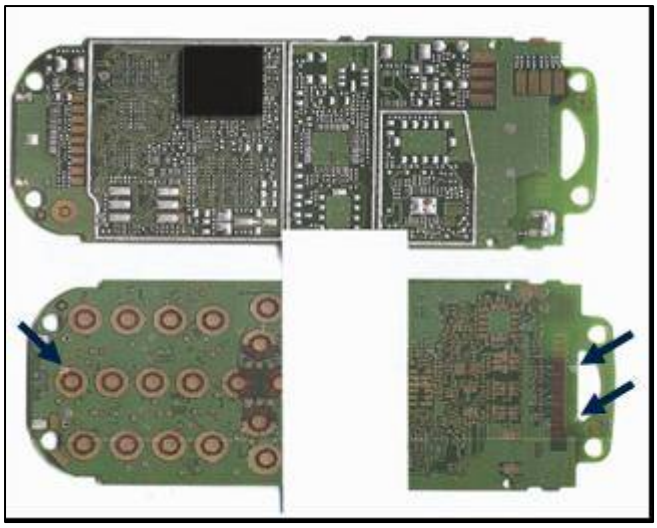

Figure 23: arrows are showing where the metallic needles contacted printed metal lines on the PCB

3.3 Process Capability & Transition Analysis

While the risk analysis described above focuses on a single process, not considering where the charging possibly comes from, the Process Capability and Transition Analysis (PCTA) looks at the process in total and analyzes whether there is charging at all, that theoretically could result in a discharge during process deviations. Additionally it looks at HBM and MM related problems as well as transitions between process steps. A detailed description can be found in [7]. It includes the following:

1. Defining the process critical path, identifying key process elements and their transition points
2. Making transition point measurements
3. Summarizing findings

3.3.1 Defining the Process Critical Path

The critical path may be defined as a series of tasks (e.g. cleaning, screening, parts addition), each of which must be completed in order to finish a product. In the following example, the process critical path starts at Receiving and ends at Shipping.

Tasks fall into two categories:

- A process function (this related to all assembly and test operations)
- Movement, i.e., transport, from one task to another.

Process **Transition Points** occur when the product undergoes a change in the process (i.e. board changes from a manual transport operation to placement on the screening conveyor). Transition points are possible sources for ESD events that require special attention during process analysis.
Figure 24 illustrates a basic process that was studied for PCTA and consists of human transport and automated equipment tasks. The process basically includes:

1. A board screening operation
2. Parts installation
3. Reflow

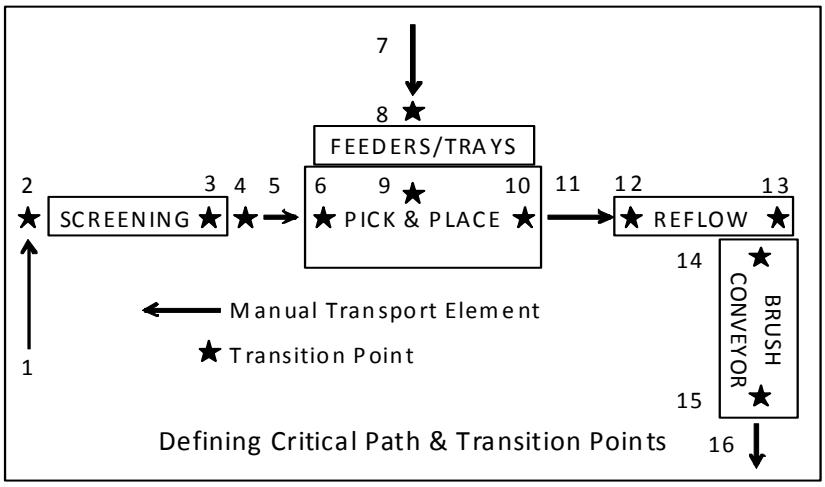

Figure 24: Characterizing the critical path and identifying transistion points

Detailed analysis of Figure 24's critical path reveals the following transition points.

1. Manual Transport of bare boards to Screener
2. Manual Load Screener
3. Screener Applies Solder Paste
4. Boards Manually unloaded & Inspected
5. Screened boards Manually Transported to Pick & Place/SMT equipment
6. Boards Manually Loaded into placement equipment
7. Devices Manually transported to Feeder
8. Devices Manually Loaded into Feeder
9. Devices Automatically transported from Feeder and installed on boards
10. Boards Manually unloaded from Pick & Place equipment and inspected
11. Boards Manually Transported to Reflow
12. Boards Manually loaded onto Reflow Conveyor
13. Boards Automatically Transported through Reflow
14. Boards Brush Conveyed from Reflow outlet
15. Boards Accumulate at end of Reflow Brush Conveyor
16. Boards Manually Removed

Once all process steps are described the next step in PCTA is the measurement of the critical Transition Points.

3.3.2 Transition Point Measurements

The objectives of transition point measurements are to assess that portion of the process for conditions that would create HBM, CDM, or MM events. Then quantify the potential magnitude of those ESD events as they relate to the ESDS device sensitivity thresholds, even if the numbers are not comparable directly.

The measurement may not reveal that an ESD event is taking place at that transition point. Rather, it may show that an assembly is being charged at that specific point in the process, only to discharge at some later time. It would also indicate how the assembly is

being charged. Proper analysis will provide the probable type of ESD event the assembly will see when and if discharge occurs.

To this end, measurements include:

1. The electrostatic voltage or charge condition of ESDS devices or subassemblies:
   a. Prior to a transitional element
   b. After the transitional element
   c. In some cases during transitional element
2. The electrostatic voltage or charge conditions and resistance to ground of equipment, personnel, operational surfaces and materials
   a. Making direct contact with ESDS devices and assemblies, or
   b. Producing electrostatic fields near or in the process flow, and at transition points
3. Identifying the charged device or object's discharge waveform

In [7] a detailed description of the new and the traditional measurements to analyse all sorts of ESD risks is given. In this section the focus is on the contribution

- of human charging to later CDM events
- of material handling devices and aids, e.g., device trays, totes, tape and reel, etc, for potential charge transfer to ESDS devices
- ESDS devices, subassemblies and their connectors to potential CDM events
- Field measurements in the critical path and inside automated equipment for FIM (Field Induced Model) assessment

3.3.3 Performing a Process Capability & Transitional Analysis

The Figure 24 process case study illustration consists of

- Five personnel transport and handling transition points
- Screening solder paste onto circuit boards
- Loading the feeder
- Placing parts on circuit boards in the Pick & Place equipment
- Reflow

The first task where the board can get charged is the **screening operation**, which consists of the following key transition points:

- The operator loads boards by hand into the screener
- The operator removes the boards after screening for inspection
- Parts are manually transported to Pick & Place (SMT)

A high impedance contact voltmeter was used to measure voltage on the board conductors before and after the screening processes (Figure 25). Voltage before screening was less than 20 volts. After screening more than 440 volts were measured on the board's conductive elements.

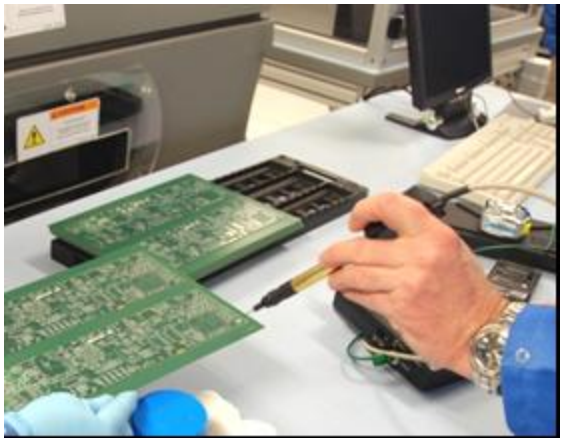

Figure 25: Measuring PC conductor with high impedance Contact Voltmeter

Screening summary indicates:

- Screening process charges board's conductive elements to >440 volts
- The charge poses a possible ESD CDM discharge source during subsequent handling or device placement if the charge is not removed
- In the illustration study, an ionizer was recommended to eliminate board voltage to reduce discharge risk later in the process

Pick & Place (SMT) Process:

At the SMT process several items require evaluation:

- Device trays, tape and reel supplied to placement equipment.
  - Are these parts charged by the materials or process creating a potential CDM event later on?
- Does the placement equipment charge the parts prior to placement on the board?
- Are there insulators in the process that may induce charge on the device or PCB during placement?

Consequently, this portion of the process must be broken into two parts: Analysis of the Feeder transition points and analysis of the placement equipment

Feeder Transition Point Analysis

The Feeder is loaded with devices that are manually transported to, and then mounted in the Feeder for delivery to the SMT equipment. Once loaded, trays and individual devices were measured with the contact voltmeter to determine existing voltage caused by transport that may not have dissipated after mounting in the Feeder.

Placement Transition Point Analysis

The placement analysis of the Pick & Place process description includes:

- Screened boards placed by hand into machine.
- Conveyor moves board into position
- Machine picks up IC and other devices and places them onto board
- Conveyor moves board to machine exit

The placement concerns include the following potential ESD issues:

- Static generators near placement (FIM)

- Isolated charged placement nozzles and other conductive objects (MM)
- Parts charged from pick up process
- Note that we previously measured the Feeder process to see if parts are charged before pickup.
- Discharge from a charged device to conductive solder paste or socket (CDM)

Equivalent Field Voltage Measurement Considerations
To assess the SMT equipment for electrostatic fields that may emanate from machine guards, plastic windows, pneumatic lines and other auxiliary materials, a special carrier (Figure 26), resembling a circuit board, can be used.

The carrier is approximately 21.6 x 27.9 cm (8.5 x 11.0 inches) and serves as transport for a portable CPM (Charge Plate Monitor) and battery operated recording device. The carrier is transported through the machine by the conveyor system, the CPM measures the field and the recording device saves the data for later viewing.

The CPM plate is 15.6 pF and will see induced voltages differently than a device. A concern is relating the measured voltages to the device sensitivity and size (capacitance) of the device. In one approach we consider the 15.6 pF plate at the midpoint of ANSI/ESD STM 5.2 CDM standard calibration references of 4 and 30 pF. However, these values do not reflect device capacitance; they are simply a reference. Actual measurements of the internal SMT equipment voltages using this special CPM were less than 12 volts.

Figure 26: Instrument carrier with portable CPM and recording device

CDM Measurement Options
Two options are apparent for measuring potential CDM problems in the SMT equipment.

One option is to program equipment to pick up a critical device and stop the placement of the device well above board placement. Then measure the device conductors with a contact voltmeter and compare measured voltage to the ESDS device's CDM damage threshold.

The second option uses the above carrier with portable CPM and recorder positioned at the point of device placement. Here the device is placed onto the CPM by the programmed placement equipment (Figure 27). Any device voltage is shared with the CPM and stored in the recorder's memory for later analysis.

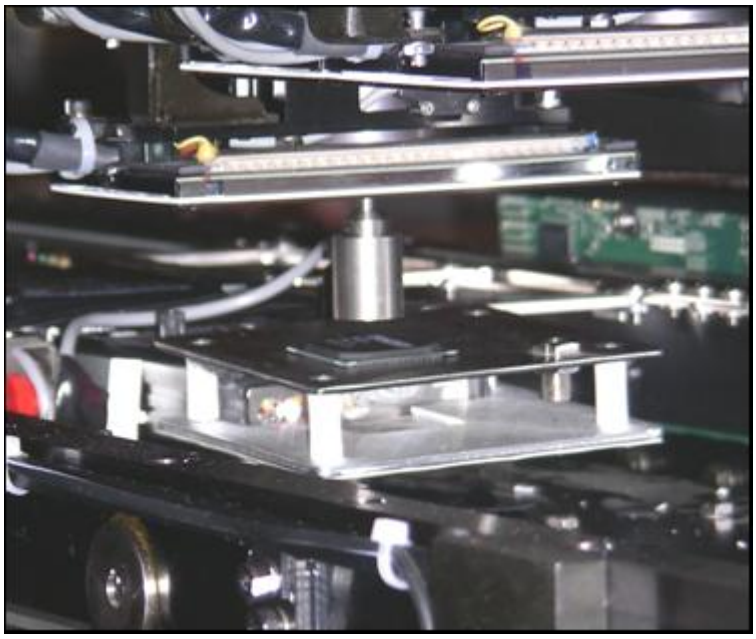

Figure 27: Device charge sharing measurements with portable CPM

The Feeder and SMT equipment analysis summary indicates:
- The feeder and the trays are properly grounded and the parts are not charged
- Electrostatic fields are not a concern. < 50 volts were measured on the CPM
- Tribocharging or voltage induction of devices due to IC handling is not a concern < 50 volts measured on the CPM at device contact

In the illustration case study the bare circuit board was charged to >440 volts at the screener. The board was not discharged and was transported by a non-charge generating person to the SMT equipment still having >350 volts on the board. At SMT output, the board voltage was >290 volts when it was transported to Reflow.

Reflow Process
The reflow process includes
- Boards manually loaded onto metal conveyor
  - Note that boards in the illustration study remained charged >200 volts

- The system includes a metal wire conveyor grounded to machine frame
- Primary concern: Are discharges occurring between charged boards and grounded metal conveyor?

- Conveyor system collects boards after reflow completed

Board Loading

Measuring board voltage with a Contact Voltmeter prior to, and after placement onto a conductive surface will indicate:

- If an ESDS assembly discharges upon contact (CDM)
- If the assembly becomes charged by the conductor upon contact (MM)

Reflow Accumulation Conveyor

In the illustration study the board exited Reflow with <10 volts on its conductors, then transitioned to a rotating brush conveyor (Figure 28). The board was transported to the end of the conveyor. The brush conveying system operates on an adjustable friction basis. If a board is stopped, friction increases and the brush stops turning, assuming it is properly adjusted. In the illustration study, the brushes continued to turn generating >525 volts on the boards awaiting manual transport to Cleaning and Testing.

Figure 28: Uncontrolled brushes generate > 500V on PCBs

Reflow analysis summary indicates

- Discharges detected at loading of reflow conveyor
  - Board was charged to 200 volts before entering reflow conveyor
  - Blow ionized air across the board prior to moving to reflow to resolve
- Conveyor at exit of reflow charging boards to >500 volts.
  - Possible discharge to grounded operators or at next process step
  - Change conveyor system or add ionization post reflow

Summarizing Process Capability & Transition Analysis Results
A basic summary of the Illustration Process Capability Analysis Study (Table IV) indicates problem areas, voltage measurements, type of potential discharge events and whether the process is within specification.

Table IV: Process Analysis Summary of PCTA Illustration Study

Process Step	Input Voltage	Output Voltage	ESD Model	Within Spec.
Screener	40	268 -441	CDM	NO
SMT Placement	216	95 – 200*	CDM/MM	NO
SMT Feeder	-0	<50	CDM	YES
Reflow	>200*	>500	CDM	NO
*NOTE: Residual Voltage from Screener Operations				

Example of CDM like failure on System level
Large controllers for hard drive data centers have many features and options that allow customers to configure what they need. In order to allow for a customizable solution the controller had to be flexible. This was accomplished by selectively plugging in PCB depending on the configuration ordered.

However, this did require the use of dummy PCBs when the features were not required to ensure that the airflow still allowed for the correct cooling of the remaining PCBs. These dummy PCB were made of an insulating plastic material without any regard to ESD requirements. These plastic PCBs were found to generate large electric fields. When using a field meter the readings could be as high as 10,000 V/in. The process at the time was to plug the dummy PCBs first and then the active logic PCBs. This caused a voltage to be induced in the logic PCBs and the first pin that made contact would take the biggest discharge. This resulted in a failure rate of up to 5% at the functional test level.

Two fixes were put in place. The first fix was very simple. Change the order of plugging so that the logic would be plugged before the dummy PCBs. The long term fix was to find a material that was static dissipative.

The result of the change in process resulted in the elimination of CDM type failures. The long term fixed ensured that even if the process was worked around, the failure could not happen.

3.4 Conclusions
Two similar methods to analyze an assembly with respect to CDM risk are described. The described examples showed how to use these methods in actual production lines.
The field problems presented showed that if such a CDM risk analysis is not performed even devices considered CDM robust may fail during assembly or testing since a board can get charged and discharges at a significantly higher current level than the stand-alone IC device at the same charging voltage level.

A risk analysis performed according to the described methodologies and – if required -the implementation of a few process specific measures enables the manufacturer to handle even very CDM sensitive devices.

References

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[2] ANSI/ESD S20.20; 2007; Development of an Electrostatic Discharge Control Program for: Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)

[3] IEC 61340-5-1; 2007; Development of an Electrostatic Discharge Control Program for: Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)

[4] Industry Council on ESD Target Levels White Paper 1: A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements, http://www.esdtargets.blogspot.com

[5] R. Gaertner, Do we expect ESD-failures in an EPA designed according to international standards? The need for a process related risk analysis; EOS/ESD Symposium 2007, pp 192-198

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[8] R. Gärtner; Field Induced CDM-Ausfall in der Halbleiterfertigung; 6. ESD-Forum 1999. München, Deutschland, pp 51-56

Chapter 4: Impact of CDM Requirements on Products

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4.1 CDM ESD Requirements

As described in Chapter 1, an understanding of CDM ESD has developed since the 1970's. Over the years, levels for CDM have been an ever changing target. As shown below in the roadmap for ESD [1] Figure 29, in the earlier years, CDM design target levels were significantly lower. As demands for improved CDM levels in manufacturing sites continued, design goals were adjusted upwards reaching levels in the mid 1990's which became unrealistic to maintain for advanced technologies. Today, an improved understanding of the manufacturing environment [2, 3] and the ever present need to push for higher I/O performance in advanced technologies have combined to push down design target levels.

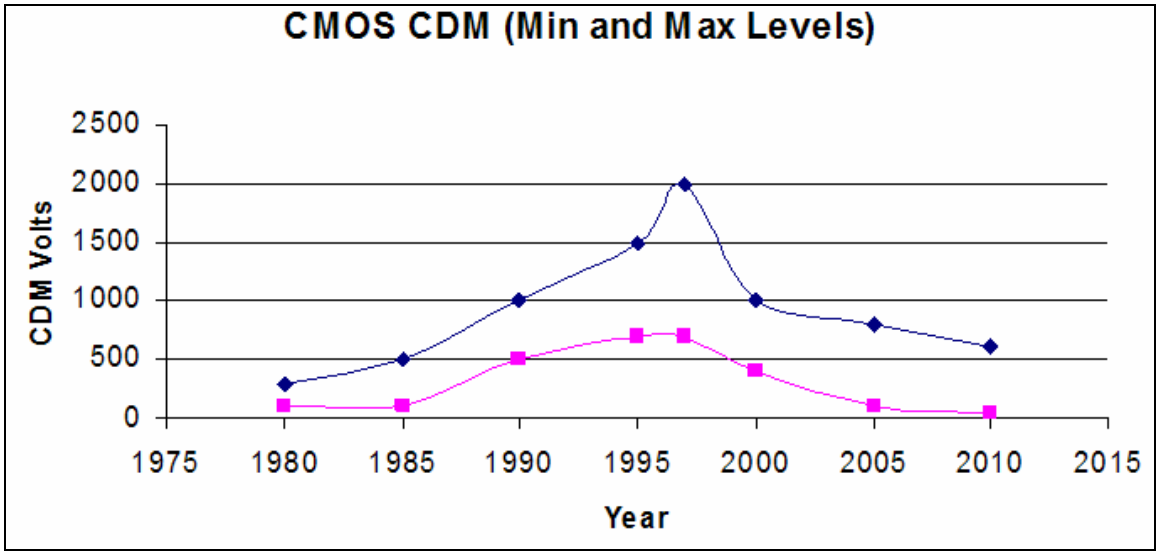

Figure 29: Evolution of CDM Design Levels vs. Time [1]

Today, most major semiconductor suppliers quote a CDM target level of 500V or less for CDM protection. But even with the reduced CDM targets, the demands of ESD protection devices create a constant chip design challenge, balancing I/O performance against CDM targets. The next section reviews the impact on current products from many major semiconductor manufacturers.

Looking at CDM ESD levels today from the customer side of the semiconductor industry, one finds a broader list of requirements ranging from 500V with many customers to as high as 750V to 1000V. Customers requesting 1000V do not appear to have a clear justification for these target levels other than organizational inertia. Some customers have no target level at all. In the automotive industry the AEC-Q100 specification still calls

out a 750V requirement for corner pins, although a separate corner pin requirement becomes more difficult to justify in today's advanced packaging. Within the Telecommunications market segment the need for high performance I/O's has dictated a much more flexible CDM ESD environment in which many customers allow significantly lower CDM target levels and are still able to manufacture these products with minimal risks.

In general, there is a wide variation within the electronic industry in regards to target levels needed for CDM ESD and over the years the acceptance levels have varied greatly.

4.2 Impact of Goals on Products

As we look closer at the impact these goals have on products, we see that it impacts both suppliers and customers. Table V summarizes some real life examples supplied from various semiconductor houses on the impact of the 500V CDM goal.

Table V: Work Effort to Improve ESD Levels to 500V

Product	Impact	Schedule delay	Effort Impact	Tech node
P1	Package modification	No	5 person months	-----
P2	ESD performance de-rated	Yes	30 person months	90nm
P3	Circuit redesign	No	10 person weeks	180nm
P4	Circuit redesign	Limited	5 person months	SOI
P5	Minor circuit redesign	Limited	2 person weeks	250nm
P6	ESD performance de-rated	Yes	40 person months	65/90nm
P7	Circuit redesign & ESD de-rate	No	18 person months	65/90nm
P8	ESD de-rate	No	5 person months	65nm
P9	Circuit redesign & ESD de-rate	No	8 person months	90nm
P10	Circuit redesign	No	9 person months	45nm
P11	Circuit redesign	Yes	10 person months	180nm
P12	Circuit redesign	Yes	12 person months	180nm
P13	ESD de-rate	No	2 person months	90nm
P14	Circuit redesign	No	30 person months	45nm
P15	Tester artifact	Minor	4 person months	130nm
P16	Circuit redesign	Yes	1 person yr	180nm
P17	Circuit redesign & ESD de-rate	Yes	4 person months	130nm

As can be seen, the impact included significant costs to the supplier in terms of work required to improve the CDM level and significant costs to the customer in regards to schedule delays. Also, in several cases, even with a re-design effort the CDM target levels were still not achieved, resulting in a lowering of the product CDM levels. This effort in many cases was unnecessary as the impact in the manufacturing environment was insignificant. More details on manufacturing environment impact can be found in Chapter 5.

Looking at this data from Table V in a slightly different way, it can be shown that this challenge is only getting worse. Moving into more advanced technologies will tend to

aggravate the risk that circuit redesign is required to meet the current target levels. This will inevitably lead to additional delays in product launches and/or more products de-rated with respect to the current CDM targets. Please refer to Figure 30 in which the work effort to improve CDM target levels is compared to the technology node.

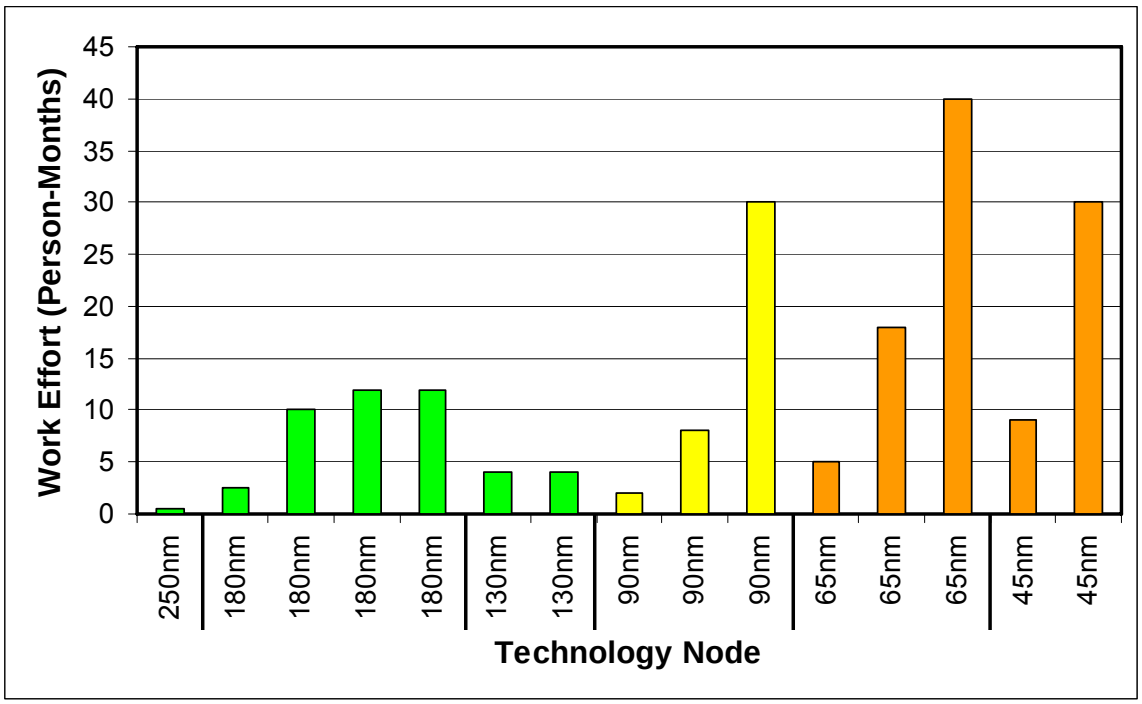

Figure 30: Increasing CDM Redesign Effort with Successive Technology Nodes. Each column represents the additional effort of a single design project to raise the CDM level above 500V

Additionally, end customers will continue to see de-rating of CDM levels for certain pins and/or pin types to be an increasing solution to the problem of hitting the current CDM target levels. As was shown in Chapter 2, this is due to the ever increasing challenge of balancing ESD protection against I/O performance. In many cases an I/O cannot meet the CDM target level without significant performance hits to the product and a negative impact on the product launch. Additionally, semiconductor houses today may routinely relax CDM goals in one of the following ways:

-Reduction in CDM target levels based on the operating frequency of the pin
-Reduction in CDM target levels based on the package size

Some of these actions are readily accepted even today in market segments where the demands of I/O performance outweigh the ESD risk. Products today have been shown to be handled with CDM target levels even as low as 50V.

4.3 Supplier / Customer Impact of a Revision to the CDM Target Levels

A reduction in the CDM ESD target level to 250V would result in a significant benefit to both the supplier and the customer:

- Elimination of a significant number of circuit redesign efforts and corresponding work effort / requalification that results
- I/O area savings with reduction in ESD protection area
- I/O performance improvements from reduction in capacitance/resistance
    - An ever increasing demand for higher IO performance can be achieved. Capacitance on IO's can be reduced by 40-50% with a reduction in the target levels
- Improvements in time to market for many products
    - Improved time to market with higher performance IO's will greatly benefit end customers

These changes would have no significant impact on the manufacturing environment.

Elaborating on the IO performance benefit and referencing again Figure 18 from Chapter 2, one can see the significant upside in the pin count of packages which can accommodate higher frequency pins. In many cases the pin count is increased by nearly an order of magnitude over a package limited by a 500V CDM goal.

References

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Chapter 5: Consolidated Industry Data on CDM levels vs. Field Returns

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Theo Smedes, NXP Semiconductors

This chapter discusses the impact of the CDM qualification level of a device on the potential risk of failure of this device in the field. The evaluation is based on the data gathered from many members of the council.

Although many members of the Council contributed with data, the total quantity of devices that was included is less than for the HBM analysis, since CDM testing is not as common as HBM testing. Nevertheless a total quantity of nearly 12 billion devices collected between 2003 and 2007 should give a good representation of the situation in the field. The device types range from discretes to ULSI system-on-chip parts. Field returns from testing and handling at the IC supplier, from the board manufacturers and from end-customers have been considered. There is a weak dependence of the return rate on CDM qualification level. Typically these returns are caused by problems in the ramp-up phase of the manufacturing process at all partners in the production chain of a new product. Minor changes in the ESD control of the manufacturing process solve these problems instantaneously without big investments. No dependency between EOS related returns and CDM levels were detected.

Real CDM failures (gate oxide failures), like those generated during CDM qualification tests, are mainly occurring in the semiconductor backend and testing, but are not included in most of the data collected.

5.1 Field Return Rates versus CDM Voltage Level

The EOS/ESD field return data of various types of products have been collected. Product types range from discretes, memory, automotive ICs, µ-processors to highly integrated system-on-chip ICs for mobile communication. The analyzed fails include mainly returns from manufacturing of the board and end-customer. About 1000 different designs are considered. The total number of shipped devices in this data base amounts to 11.6 billion. The returns are analyzed versus the CDM withstand voltage of the design since this could give a correlation to the charging voltages measured in the field and since qualification test results are reported in voltage. Since the number of devices in the different voltage classes are not equal, the failure rate was statistically weighted (using the ChiINV function [1]) to get an indication about the possible expected upper failure rate limit with a confidence level of 60%. By doing this the different voltages classes can be compared much better. Figure 31 shows the statistically expected maximum failure rate as a function of the CDM withstand level.

In general, the analysis of the data was hindered by the fact, that

- Different CDM standards (JEDEC and ESDA) were used.
- In many cases the fail level was not determined, instead only tested up to 500V to confirm meeting a target. Thus, the actual withstand level might be much higher. This especially applies to parts passing 500V.

The inspection of Figure 31 shows a drop in the failure rate at a withstand voltage of 500V. This could lead to the assumption that a minimum CDM robustness of 500V is needed for a safe handling. However, a more detailed analysis of the data reveals, that the statistics in Figure 31 are dominated by very high failure return rates (> 100 returned parts) of 15 designs out of 949. If these are excluded, there is a more or less equal distribution of FARs observed across the CDM robustness classes as shown in Figure 32. This applies to 934 designs and 9.5 billion shipped devices. The return rates are clearly below 1 dpm.
It is also evident that notable returns rates can even be found with passing CDM levels of >1500V.

The few designs with higher failure return rates (> 100 returned parts) resulted from EOS-like events as shown in Section 5.2.2. A relation to a CDM like discharge event could not be shown.

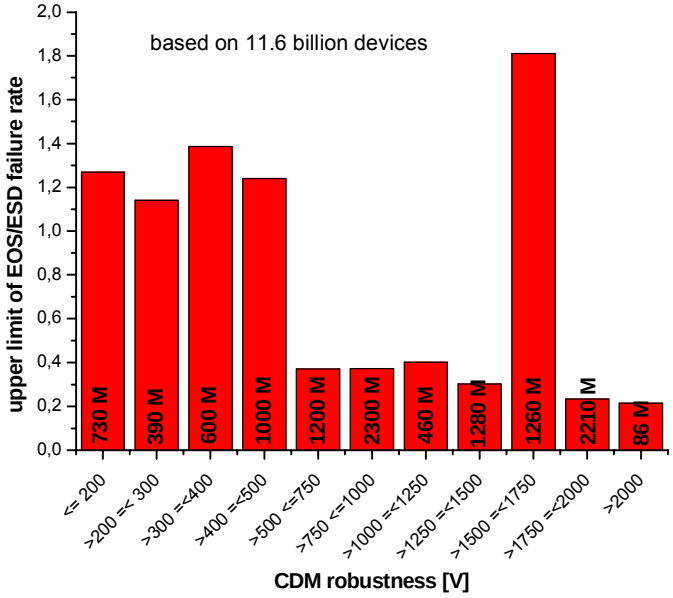

Figure 31: Upper limit of EOS/ESD failure return rate (in defects per million) versus CDM withstand voltage. An amount of 11.6 billion shipped devices has been considered. The number of devices shipped within a certain CDM classification regime is noted in each column.

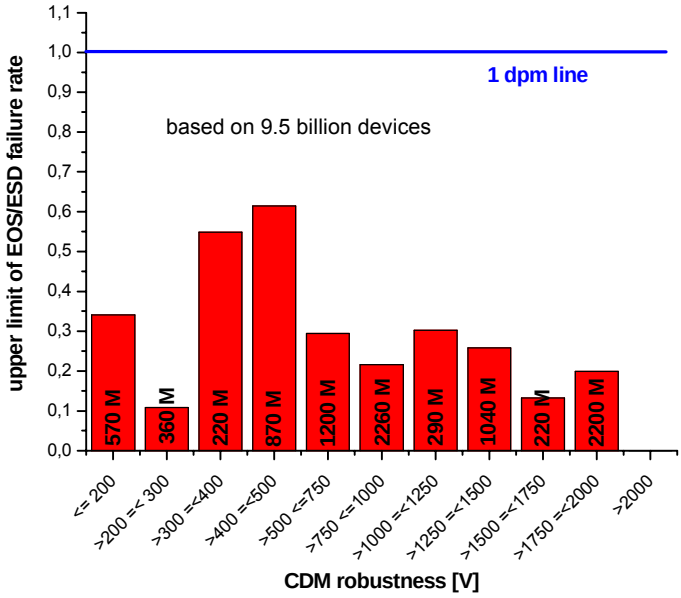

Figure 32: EOS/ESD failure return rate (in defects per million) versus CDM withstand voltage. Same data base as Figure 31 but any designs with clearly elevated return rate (> 100 reported fails) have been removed.

5.2 Analysis of Typical Examples

5.2.1 Typical CDM-like Failure Picture

Figure 33 is taken from an FA report of a device with high speed IO pins having a low CDM value (< 125V). The failure found in the field (semiconductor fab) shows exactly the same failure signature as devices damaged during CDM qualification testing.

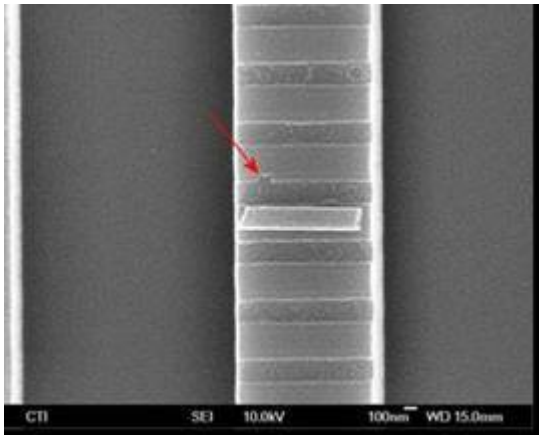

Figure 33: The SEM micrograph of the FAR depicts a pin hole in a gate oxide. This failure picture is classified as typical CDM-type fail.

But failures with such a typical CDM qualification test failure signature are very difficult to find. Most of these occur during manufacturing or testing at the semiconductor manufacturer's site.

5.2.2 Typical EOS-type Failure Picture

The collected EOS/ESD failures include all types of EOS related failures (including system level ESD) and ESD related failures (including CDM-type failures). Usually HBM related failures are rarely observed [2]. Comparing the subset of designs accounting for 1.6 billion sold devices indicates that most of the EOS/ESD fails are due to electrical overstress (EOS).

Different from typical CDM failures, indicated by little pin holes in the gate oxide, most of the field returns show large areas of melted metal like in Figure 34. This example is taken from a device mounted in a TQFP 100 package which showed 409 fails out of 36 million sold devices. It is one of the outliers of Figure 31 depicting a very high CDM robustness (1000V). A typical EOS-type failure of a melted metal bus was found. This implies a large amount of dissipated energy. The comparatively lower energy of a CDM event is not able to generate such an extended failure signature.

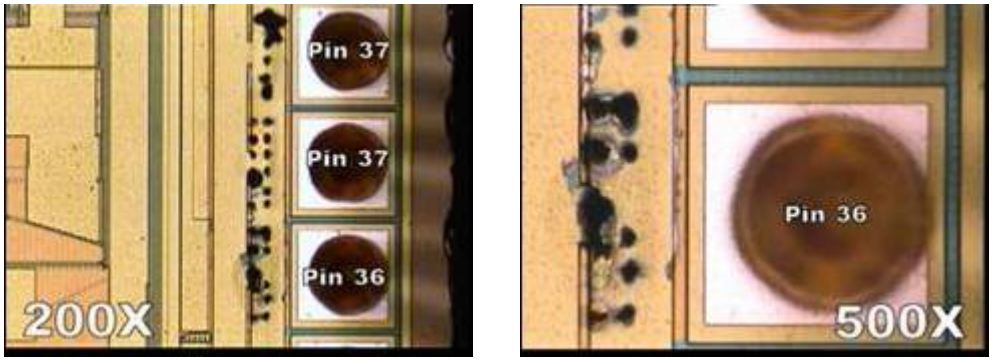

Figure 34: By optical inspection FAR depicts major damage in the metal bus which is an indication of a large amount of dissipated energy. This is rated as a typical EOS-type fail.

Another example of an EOS type failure was found with a large device in a LGA 1681 package as shown in Figure 35. The device had a reasonable CDM robustness of 300V determined by its 320 High Speed pins. All other pins had a CDM robustness of more than 500V. The failing devices coming back from customers did not show failures on the High Speed pins. Only on power supply pins with a much higher CDM robustness were affected. As can be seen in Figure 35, the failure analysis showed a junction punch through which cannot be generated by a CDM like event but only by an event with a higher energy, i.e. an EOS like event.

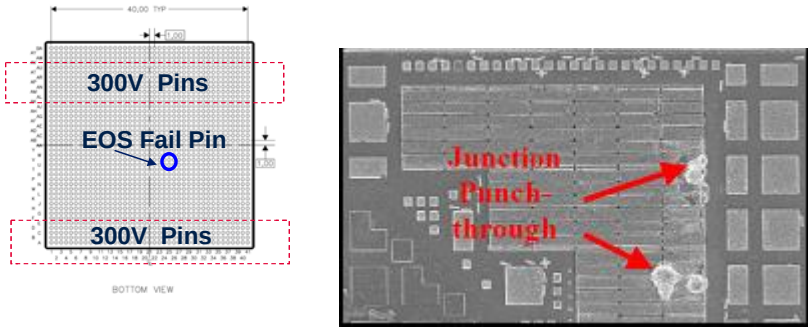

Figure 35: EOS-type damage that happened on the more CDM robust power pins of a device and not on the weaker High Speed pins.

5.3 Conclusions

The FAR data of more than 11 billion devices collected by the members of the Council showed that EOS/ESD failures can appear in the field independent of the CDM robustness level from less than 100V to greater than 2000V.

During CDM qualification testing, the typical failure seen is a dielectric breakdown. Such a failure is mainly seen at the IC supplier during the ramp-up phase of a new product with low CDM robustness. This can easily be solved by improving the ESD control measures without doing a redesign of the product. Usually only a minor effort combined with a low investment is required.

Case studies showed that most of the field failures in the FAR data are due to EOS or Charged Board events. These EOS like failures normally did not occur on the CDM weak pins but on more robust pins that are somewhat exposed. Also, these CBE like failures are not directly comparable to CDM like failures. They have their origin in the charging of the board which can be assessed in the same way as “real” CDM like failures.

References

[1] Chernoff H., Lehmann E.L. The use of maximum likelihood estimates in $\chi 2$ tests for goodness-of-fit. The Annals of Mathematical Statistics 1954; 25:579-586.

[2] White Paper 1 ‘A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements’ Industry Council on ESD Target Levels, August 2007

Chapter 6: Recommendations for Realistic CDM Target Levels for the Present and an Outlook for the Future

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Reinhold Gaertner, Infineon Technologies
Charvaka Duvvury, Texas Instruments

6.1 Preface

In the preceding chapters, control of the manufacturing environment to prevent CDM events and design of ESD protection addressing CDM parameters has been discussed.

In contrast to HBM, there is no single CDM measurement parameter which relates to both CDM testing (Appendix C) and CDM ESD design (Chapter 2), or to evaluation for CDM control measures (Chapter 3). HBM voltage levels allow both the extraction of a current level sustained by the ESD protection design and the corresponding voltage which can be correlated to measured voltages in the manufacturing environment, providing a useful guide for the quality of the ESD control measures. In contrast, the correlation between current and voltage levels in a CDM tester varies widely with the size of the package itself, the applied test standard and the ambient conditions during the test.

As in the case of HBM, the application of ESD control measures in the EPA guarantee a safe manufacturing of parts passing a base ESD level. For CDM, fails might occur even for parts with extremely high "CDM robustness." This can only be corrected by an audit of the process steps and introduction of process specific control measures. These details are covered in Chapter 3. For example, Table III in Chapter 3 lists possible risks in the PCB assembly. This is an illustration that CDM reliability does not just come from products with a specific CDM level but that manufacturing control measures are equally important. This CDM process control audit / process specific control is typically not a relevant cost factor.

As a consequence, a **compromise** has to be found incorporating growing limitations of the on-chip ESD circuits as well as a major effort in the ESD control field. The intention of this chapter is to propose a CDM target which accommodates both constraints without compromising quality. Moreover, we also present a realistic roadmap for CDM as the technologies further scale into deep sub-50nm nodes towards 22nm and beyond.

6.2 Relevance of Current Level

The CDM damage mechanism is typically due to an excessive on-chip voltage drop caused by the CDM peak discharge current. Thus, all on-chip design measures address the avoidance of this excessive voltage drop at critical locations such as across thin gate oxides. The sizing of the protection clamps is based on the value of the peak current level which has to be safely passed. In the CDM domain, this peak current level can exceed the

HBM peak current by an order of magnitude. In the case of IO ESD cell development, it is not known beforehand which package they will be used in, yet the package is a major contributor to peak current. Thus, a well-defined current level is critical as a design goal.

6.3 Relevance of Voltage Level

The relevance of the CDM voltage levels comes from the gathered experience of ICs manufactured at production lines around the world, where only the CDM voltage level of the qualification test is known. The drawback is the deviation between the various test standards as discussed in Appendix C.

6.4 Correlation to Control Measures in Manufacturing Environment

The correlation of the CDM qualification voltage level of an IC to the capability of handling it in an EPA is of empirical nature. The measured voltages in the line and the tester pre-charging voltage have no direct correlation. It is also unclear whether the strong dependency of the damaging current on the package, as given by the CDM tester, also appears in the real world events within the manufacturing site.

Based on the experience of handling parts of a certain robustness class, analysis methods have been developed to rate the quality of an EPA concerning CDM events as described in Chapter 3.

6.5 Recommended CDM Target Level

If a detailed process specific assessment of the manufacturing, handling or testing process is performed by an ESD control expert applying the available measurement methods (Chapter 3), a safe manufacturing environment, both during ramp-up and volume production, is guaranteed even for parts with CDM withstand voltage < 125V. This is an ideal case. But knowing that the capability of a detailed CDM assessment is limited today, we recommend reducing the audit effort while still maintaining the basic CDM control measures for products with CDM level of 250V and above. For products with CDM levels between 125V and 250V some extra effort, beyond the basic CDM control, is needed. This should ensure that proper CDM qualification is practiced for different classes of devices as listed in Table VI below.

Table VI: Realistic Rating of CDM ESD Qualification Levels for All Package Types

CDM classification level (tested acc. to JEDEC)	ESD control requirements
$V_{CDM} \geq 250V$	• **Basic ESD control methods** with grounding of metallic machine parts and control of insulators
$125V \leq V_{CDM} < 250V$	• **Basic ESD control methods** with grounding of metallic machine parts and control of insulators + • **Process specific measures** to reduce the charging of the device **OR** to avoid a hard discharge (high resistive material in contact with the device leads).
$V_{CDM} < 125V$	• **Basic ESD control methods** with grounding of metallic machine parts and control of insulators + • **Process specific measures** to reduce the charging of the device **AND** to avoid a hard discharge (high resistive material in contact with the device leads) + • **Charging/discharging measurements at each process step**.

However, one must note that if a detailed process specific assessment is not done during **ramp-up**, production failures can still occur under some rare circumstances for products **with any CDM level**. In this case a specific audit is needed to find the root cause of the failure and to remove it by process specific control measures.

Impact of the Recommended CDM Target Level

Technology downscaling combined with increased IC performance requirements and the trend towards larger package sizes have all placed severe constraints for CDM protection design. It has now become apparent that a 500V specification cannot be met for many products because of:

- High speed circuit requirements.
- Continued technology scaling effects closing the ESD Design Window
- Prevailing trend for high capacity IC packages

For the design of high speed circuits incorporated in large product packages, a value of 250V has proven to be a realistic design target. Parts with such a CDM robustness level are now routinely and safely handled.

While control methods to handle parts with 250V CDM and lower are available for use in a manufacturing site, there is no need to specify different CDM qualification targets for various product families. To avoid time-consuming alignment between the supplier and the customer, a general target for all products is recommended.

Therefore, the Council recommends **adopting a general CDM qualification target of 250V (tested according to JEDEC) at this time** as a reasonable compromise between on-chip design and a uniform manufacturing process control requirement for all IC products. The implementation of a higher CDM robustness in cases where it does not degrade performance or delay time-to-market adds further margin and is always beneficial.

This recommended target level is not determined by any distinct threshold found in the field returns statistics, any physical models, or ESD control standards. It has to be considered as a guiding value to allow alignment of practical ESD control measures in the manufacturing lines and ESD on-chip protection design**.** As discussed in Appendix D the robustness of these parts regarding other failure mechanisms like EOS, CBE or system level ESD is not degraded by this recommended target level.

6.6 Outlook and CDM Roadmap from Silicon Technology Scaling

As discussed in Chapter 2, the IC designs continue to place severe restrictions on the achievable CDM levels as the demand for circuit speed increases. This document has already shown that CDM withstand voltages must be relaxed to accommodate today's advanced process technologies and high speed performance requirements. For technology nodes of 65nm and 45nm, the proposed realistic goal of 250V CDM is not only safe; it is also practical and compatible with high speed IO circuit performance. This is especially true for large pin count ICs that contain these high speed macros. But as silicon technologies advance further into the deep sub-50 nm regime towards the 22nm node and beyond, even lower withstand voltages will be required to account for the scaling effects and the continued drive towards higher circuit speed performance at data rates reaching 40 Gb/sec or more. This was already indicated in Chapter 2, where we projected that starting at the 22nm node for HSS and RF, CDM levels of 125V would hardly be achieved. We therefore envision that within the next 5 years, CDM levels into the ~125V range could become the new practical targets.

A roadmap based on this projection is shown in Figure 36 below. During the early years of CDM awareness, customers requested protection levels of 1000V or 750V. For instance, during the 1991 time period AT&T specifications were 1000V for corner pins although some allowance was given to high speed pins. At the time these specifications were based on the commonly available control for CDM at the production areas. However, by the late 90s, 500V became the default standard for the industry as customers and suppliers had become comfortable with this as a reasonable level. Therefore there has been a precedence that over time a revised level is necessary to avoid over-design and avoid harsh product requirements.

With the new information presented in this document the 250V level is recommended as the safe and practical level to accommodate the design demands while noting that the CDM control methods available easily support this recommendation for all existing products. As the roadmap further projects below, within the next 5 years as the technologies approach the 22nm node, this would invariably lead to 125V as a new practical CDM level. Also, indicated in Figure 36, is the progress of CDM control within

the production areas. CDM control to less than 50V has already been demonstrated with proper advanced methods. As a consequence, "**Continuously Improved CDM Controls**" in the production areas must not only become a routine practice; it should be the primary approach to ESD sensitivity solutions. While the on-chip protection should always ensure some minimum background protection, ESD control methods should take on a more prevalent role. Judging from the expertise and the factory control methods that are available today, this would not and should not be an issue. The continuous improvement in CDM control in the factory took on a multi-faceted approach to achieve these goals. This involved an increased awareness of CDM in the production and handling areas, improvements in, and greater attention to, auditing programs along with more readily available CDM data. When leading edge devices are introduced, the response time with failure-driven process control has to be improved. In the future, additional detection and monitoring technology may also become important. The purpose of this road map is to enhance this awareness and point out the dire necessity for continuous improvement of the CDM control programs.

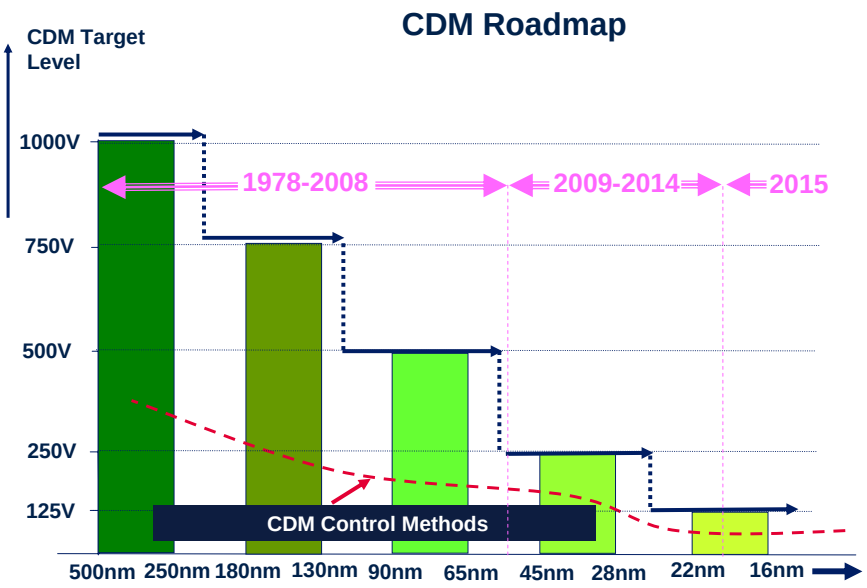

Figure 36: Evolution of CDM Target Levels vs. Time. The continuous improvement in the CDM control at the factory level is also shown in conjunction with CDM level roadmap

It should also be pointed out that the trend for CDM target levels in Figure 36 is separate from the Technology Roadmap established by the ESD Association (previously discussed in Chapter 4, Fig. 29) as shown below which represents the evolution in design levels [1].

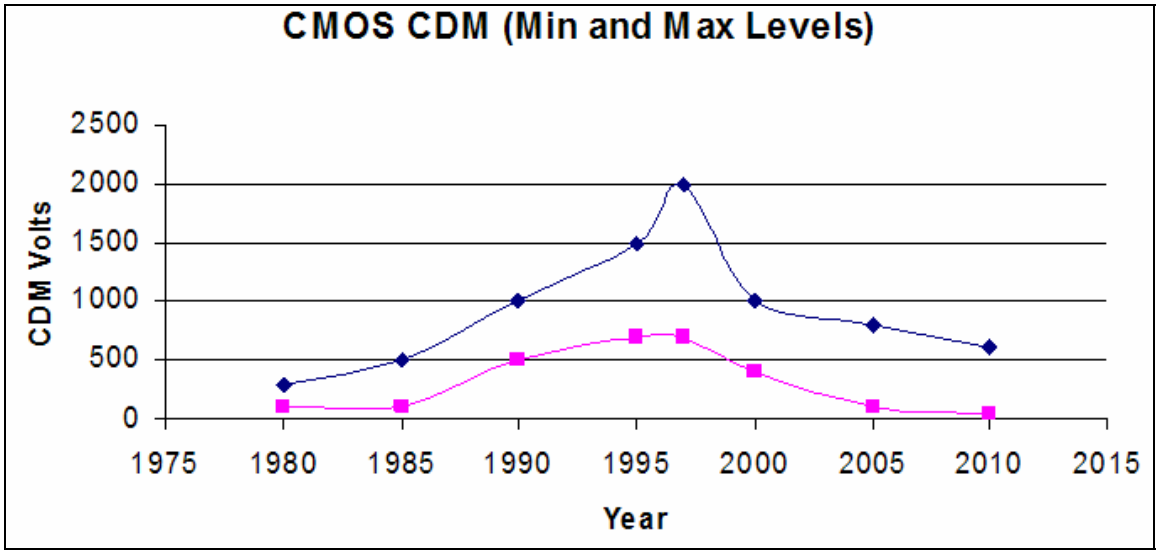

Figure 37: As already shown in Chapter 4 the Evolution of CDM Design Levels vs. Time Peaks around 1997 and has been dropping since then [1].

In Figure 37, the minimum and maximum possible practical design levels are indicated. Therefore, while even in some advanced technology nodes it is possible to continue to design for 500V, most of the circuit design cannot tolerate this level and some circuit requirements may approach levels as low as 50V. These trends are important to note as they allow the contract manufacturers to become aware and plan their development. According to this roadmap it would be judicious to make control programs aimed at the 50V level and expand them to a larger base of production areas across the world.

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[1] ESD Association Road map: http://www.esda.org

Appendix A: Some Aspects of CDM Tester Circuit Modelling

Timothy Maloney, Intel Corporation

Summary – Charged Device Model (CDM) non-socketed ESD testers as specified by ESD Association and JEDEC produce waveforms in devices and calibration fixtures that can be understood through circuit models. At frequencies up to 1 GHz or so, waveforms are simple enough that the very simplest lumped series LRC model can be used to describe the behavior. Simple extensions of the model, to consider distributed transmission line effects for both the CDM test head and the device or fixture being tested, allow many reported high-frequency (e.g., 3 GHz) features to be explained and calculated. For the basic LRC model, peak currents are calculated and plotted in the L-C plane for typical values of spark resistance as well as L and C for CDM testing of semiconductor components. This highlights and explains some key differences between the ESDA and JEDEC CDM testers. Throughout the analysis, the Laplace transform viewpoint, and its related circuit modeling methodology, is useful in transferring between the time and frequency domains. Such analysis also provides enlightening ways to look at methods proposed to duplicate the main features of CDM testing on silicon with wafer-level testing.

A.1 Introduction

The non-socketed CDM (ns-CDM) tester, according to [1, 2], can be circuit modeled as in Figure A1 and the immediate charge packet Q_{imm} can be calculated. In Figure A1, Cfrg is approximately the capacitance from the ground plane to the field plate. Cf is the capacitance of the device under test (DUT) to the field plate, and Cg is the capacitance of the top ground plane to the DUT. A CDM event happens when the discharge pin makes contact with DUT, thus closing the switch. The resulting Q_{imm} is

$$Q_{imm} = Vf\left[\frac{Cf}{Cg+Cf}\right]\left[Cg+\frac{Cf*Cfrg}{Cf+Cfrg}\right] = Q_1 + Q_2. \quad (1)$$

The effective capacitance C_{imm} thus satisfies the relation $Q_{imm}=C_{imm*}Vf$. This circuit model has shown close agreement with charge packet measurement done through the 50-ohm line shunting the 1-ohm disk resistor.

The equation above can be simplified without altering the sum if certain conditions hold. Usually, because of the thin dielectric, Cf >> Cg, which implies that Q1 << Q2. It also means the quotient Cf/(Cg + Cf) ≈ 1. We are left with the following equation

$$Q_{imm} \cong Vf \cdot (Cf \parallel Cfrg). \quad (2)$$

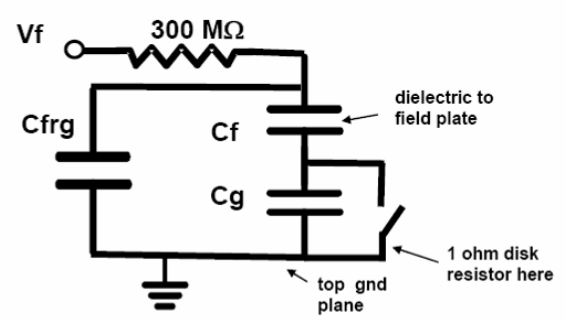

Figure A1: Circuit model for a field-induced ns-CDM tester. Switch closes when the discharge pin hits the DUT.

A.2 CDM Tester Model

The essential ESDA or JEDEC ns-CDM test circuit can be modeled as a single LRC series loop as long as certain parasitic elements are negligible. Let us first look at a more complete, yet simplified model for the CDM tester.

Various references on CDM testers [1, 3-4] have shown the utility of a 3-capacitor model of the device in the tester, and that a series-parallel combination of the three capacitors can be used to extract a single equivalent device capacitance C_{imm} for the resulting fast event. Then for field plate charge V_0, the immediate charge is $Q_{imm}=C_{imm}V_0$. The main resistive element in the circuit is the spark resistance Rs, which can vary considerably and is also time dependent [5], but a typical deduced value for the CDM tester might be 25 ohms. That leaves the inductance, which appears mostly in the test head pogo pin probe [5] and the packaged device itself. In order to match the required waveform, the JEDEC CDM test head has extra electrical length, either because of an inductor, or because the 1 ohm current detecting resistor, feeding the 50 ohm scope cable, is recessed behind a small cavity. Also, the packaged device can have up to 2-3 cm of trace length from the pin to the die for large packages. Signals on these traces may be impedance matched to 50 ohms all the way to the die, but in the ESD regime, diodes or other highly conductive protection devices turn on and reduce the terminating impedance to low numbers of ohms. Thus we have nearly-shorted transmission lines on either side of the spark resistance and switch. Before returning to the transmission line model, let us picture those 1-ohm-terminated transmission lines as equivalent T-networks as shown in Figure A2, in order to focus on the principal RLC poles and zeros of the network.

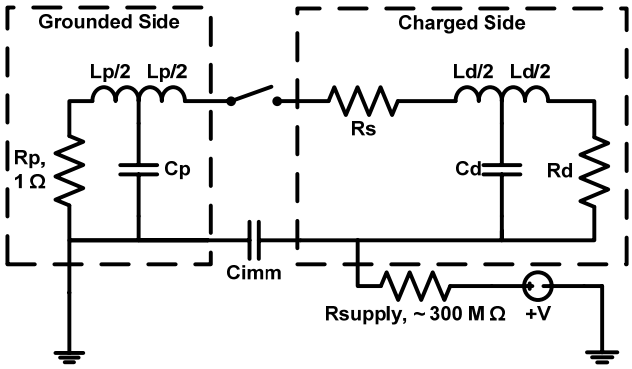

Figure A2: CDM tester equivalent circuit, with (charged) device circuit on the right and (grounded) test head and probe on the left. Rp = 1 ohm is the test head current detector and Rd ≈ 1 ohm is the on-chip protection.

In Figure A2, the charged (hot) side, with the device model, is on the right and the grounded side, with the pogo pin and test head model, is on the left. The related approximate values of Cp and Lp for package options, calibration fixtures and test head options are shown in Table A-I. Our principal concern is the outer loop of Figure A2, which is reducible to the well known series LRC. It has two poles and a zero in the admittance function, and resistance dominated by the spark. This admittance function is

$$Y(s) = \frac{Cs}{LCs^2 + RCs + 1}, \quad (3)$$

where the L,R, and C values are clear from the totals in the outer loop.

The usual observation, particularly on oscilloscopes of 1 GHz bandwidth or less, is of a single sharp spike and limited or nonexistent ringing, indicating an overdamped or slightly underdamped solution. This is the outer loop current through the 1 ohm detector. But note that the effective capacitances of the transmission lines form inner loops, all with the same resistor Rs, on each side of the circuit. This introduces several options for high frequency poles, as the device or probe capacitors bypass some of the outer loop inductance. These new poles are manifestly at higher frequency than the outer loop because of the lower inductance, and the series capacitance with C_{imm}. Thus we have the high-frequency ripple and double peaks that have been reported when multi-GHz measurement systems are used [6], and not seen for lower-frequency measurements where the outer loop alone is visible. Figure A3 is a scope trace from Ref. 6, showing these features. Note that all of these complex resonant frequencies depend on the interaction between the test head and the device under test; if the device trace length is changed, all the poles will move. Thus it is no surprise that peak currents (and much else) vary with package location [7], even aside from the C_{imm} variations due to field plate and ground plate movement. As the calibration fixtures each have few parasitics of note, and a stable C_{imm}, they should work as intended for checking out the CDM events.

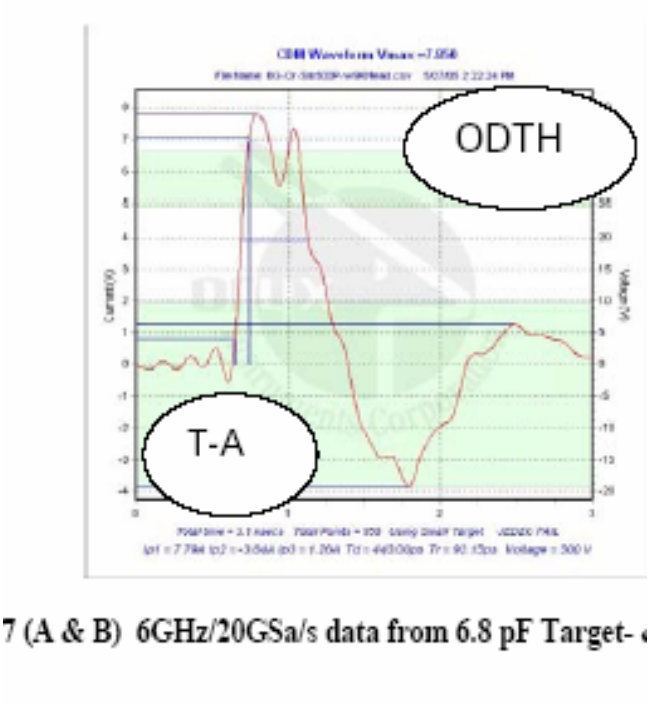

Figure A3: JEDEC CDM pulse measured with high speed oscilloscope, sensitive to higher natural frequencies and thus showing double peak. From [6]. Figure A2 or Figure A4 circuit models can explain.

The entries in Table A-I for Figure A2 also make it clear why there are occasional problems with devices tested on the JEDEC CDM test head of note—the longer electrical length in JEDEC creates higher parasitic inductance and capacitance than the ESDA head. This lowers the outer loop frequencies a little, but those are already heavily modulated by C_{imm}. This test head affects the inner loop frequencies because of its higher Lp and Cp. Note also that a loop through Cd can have low frequency for a long enough package trace, which should even have an effect on use of the ESDA test head.

The admittance zeros of Figure A2 should be noted along with the poles. The two zeros are easily seen as the parallel LC tank circuits on the right and left, corresponding to quarter-wave shorts in the associated transmission lines. Stopping the current with a zero in the admittance function may not seem to be a bad thing, but both the 1-ohm detector resistor on the left, and the protection device on the right, is in the midst of those tanks. Thus each will feel some current at its own LC tank resonant frequency, even though overall current is low due to cancellation in the tank. This means that there could be detector current that is not felt at the device and vice versa. But note that the package resonance of a long 50-ohm trace in dielectric, 2 cm as described in Table A-I, would be below 3 GHz (Table A-I is for well below quarter-wave frequency; 2 cm when dielectric $\sqrt{\varepsilon_r}$=1.5 is quarter-wave for 2.5 GHz). This is below the 3 GHz frequency reported in [6] to be the JEDEC test head resonance, so it appears that between 2.5-3 GHz we have a vigorous half-wave series L-C resonator, which could easily cause destruction. Now, let's return to the more accurate transmission line model.

Table A-I: Approximate values of circuit elements as pictured in Figure A2.

	Lp, nH	Cp, pF	Ld, nH	Cd, pF
ESDA test head	3.6 nH	0.22	x	x
JEDEC* test head	10-12	~0.5-0.6	x	x
Calibration fixture	x	x	small	small
Device, short trace (2mm)	x	x	0.5	0.2
Device, long trace (2 cm)	x	x	5	2

*JEDEC test head with 1-ohm detector resistor is recessed behind a short high-Z cavity; effective electrical length of the pogo pin probe and cavity is 2.5 cm in air, or 3 GHz resonance [6].

The CDM test system is well modeled by a loop as pictured in Figure A4, with two transmission lines in series, terminated by low-Z in each case. One line is for the device (impedance Z_{d0}, usually 50 ohms, with propagation constant and electrical length given by k_d), and one is for the test head and probe (Z_{p0}, k_p), with a presumed average test head impedance, upwards of 100-200 ohms depending on the test head. As a further refinement, the probe and test head section could be modeled as two or more line segments if needed.

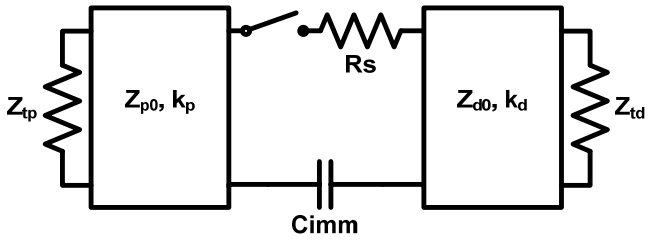

Figure A4: Generalized transmission line model for CDM test system; test head and probe side on left and (charged) device side on right.

Terminations Z_{td} and Z_{tp} are generalized forms of Rd and Rp from Figure A2. The general expression for Z_{din} is

$$Z_{din}(s) = Z_{d0}\left[\frac{Z_{td} + Z_{d0}\tanh(k_d s)}{Z_{d0} + Z_{td}\tanh(k_d s)}\right], \quad (4)$$

and there is a corresponding expression for $Z_{pin}(s)$. The admittance function for the network becomes

$$Y(s) = \frac{1}{R_s + Z_{din}(s) + Z_{pin}(s) + \dfrac{1}{C_{imm}s}}. \quad (5)$$

Clearly, the zeros of this function (aside from the usual s=0 for series LRC) occur when one of the lines goes through a singularity and we have $\tan(\pi/2)$, i.e., quarter wave resonance on a line. The poles occur when the expression in the denominator goes to zero, and the lowest frequency poles are our outer loop of interest. Because s is a complex frequency, $\sigma+j\omega$, it is important to note that these lowest frequency poles could be real and negative (overdamped), as the negative s-dependent terms balance Rs. The

events in standard CDM testers will have major real components in their lowest frequency poles as a result of the short duration and subdued ringing of the pulse.

The higher-frequency poles of Y(s) will occur beyond the first quarter-wave resonance, when one Z_{in} goes negative and (largely) imaginary, and eventually joins with the ever-smaller C_{imm} term to balance the other Z_{in}. This will happen at the lowest frequency when both Z_{in} functions approach quarter-wave near the same frequency; when one moves beyond $\pi/2$, goes negative $j\tan\theta$ and soon zeros out the denominator. Reducing the electrical length of one line pushes out this pole (or conjugate pair of poles, most likely) to higher frequency, but not above half-wavelength for the longer line. This higher frequency pole resonance can be destructive because the termination current (i.e., across our protection device) is raised by the high (equal and opposite) voltages appearing across both lines in series L-C resonance. It should be much more destructive than anything felt by the termination at a zero of Y(s). The lesson for CDM testers is that the electrical length (k_p) of the test head and probe pushes the half-wave resonance to lower frequency due to the combination of the test head and device. But since the package trace effect is part of the intrinsic factory CDM event, the high-frequency stress appears to be appropriate when those package conditions exist.

Solving Eq. 5 for all relevant complex roots and inverting to the time domain would be very revealing, but will have to be the subject of a future study. We shall now return to Eq. 3, our basic low-frequency LCR loop, for insight into our CDM testers and measurements.

A.3 Waveform Analysis

The admittance function of Eq. 3 is solved to give two poles, expressed in pole-zero form in the Laplace domain as

$$Y(s) = \frac{s}{L(s+a)(s+b)}. \quad (6)$$

In general, the poles at -a and -b are complex frequencies. These poles are given by

$$a,b = \frac{R}{2L}\left(1 \pm \sqrt{1 - \frac{4L}{R^2 C}}\right), \quad (7)$$

where the solution is overdamped if $R>2\sqrt{(L/C)}$. The sign convention is chosen so that the time domain solution will be a sum of complex exponentials e^{-at} and e^{-bt} according to Laplace transform analysis [8]. Another expression for the poles is

$$a,b = \omega\left[-D \pm \sqrt{D^2 - 1}\right] \quad , \quad (7a)$$

where damping factor $D=RC/(2\sqrt{LC})$ and $\omega=1/\sqrt{LC}$.

The CDM discharge current in the Laplace domain is I(s) = V(s)*Y(s), where V(s) is a step function for the switch arc, expressing the discharge of C_{imm} to zero. This could be an infinitely abrupt step function V_0/s, but we would like to build in the finite rise time of the spark itself, irrespective of any LCR-related rise times. This is believed to be 50-200 picoseconds (10-90% rise time), which we will capture as an additional pole so that the step has a gradual exponential approach, $V_0(1-e^{-ct})$, c positive and real. For a 10-90% rise

time τ we must take c=2.2/ τ. Our source becomes V(s) = V_0/(s(s+c)) (neglecting normalization factors) so we now have

$$I(s) = \frac{V_0}{L(s+a)(s+b)(s+c)}. \quad (8)$$

This 3-pole model should give the discharge current waveform for the basic LCR loop; this can be carried out by using methods of finding inverse Laplace transforms as in [8]. But at present, we're guessing and curve fitting to obtain resistance and spark rise time. In the discussion of peak current that follows, for simplicity we will revert to the two-pole model that is based only on single values of L, C, and R. The peak current I_{peak} for a series LCR network with initial condition V_0 across capacitor C, and perfect switch closure (i.e. 2-pole solution), depends on whether the solution is overdamped, D>1, or underdamped, D<1, D again the damping factor. The general expression is

$$I_{peak} = \frac{2V_0}{R} D \exp\left(-\frac{D}{\sqrt{\pm(1-D^2)}} \tan(h)^{-1}\left(\frac{\sqrt{\pm(1-D^2)}}{D}\right)\right) \quad (9)$$

where the $\tan^{-1}$ and + sign refer to underdamped. Figure A5 shows how I_{peak} approaches V_0/R as D increases. In Figure A6, values of I_{peak} are plotted in the plane of L and C for 500V and a value of R, 25 ohms, that is commonly found for equivalent spark resistance [9]. The overdamped case is shown in red in the region at the lower right.

For an ESDA or JEDEC CDM test reduced to this equivalent LCR, the capacitance is C_{imm} and the inductance depends on both the component or fixture being tested, and the test head. Figure A6 points out zones of general agreement with the JEDEC and ESDA tests for cases where the object being tested does not add much extra inductance to the test head, e.g., a component's Vss or Vcc plane being zapped. Note that while the JEDEC test head lowers the frequency of higher-frequency modes, as pointed out earlier, the peak current due to the principal LCR loop is actually a little lower for JEDEC due to the higher inductance. Thus the ESDA failure voltage can be lower simply due to the higher I_{peak}, if high frequency resonance effects are unimportant for the device under test.

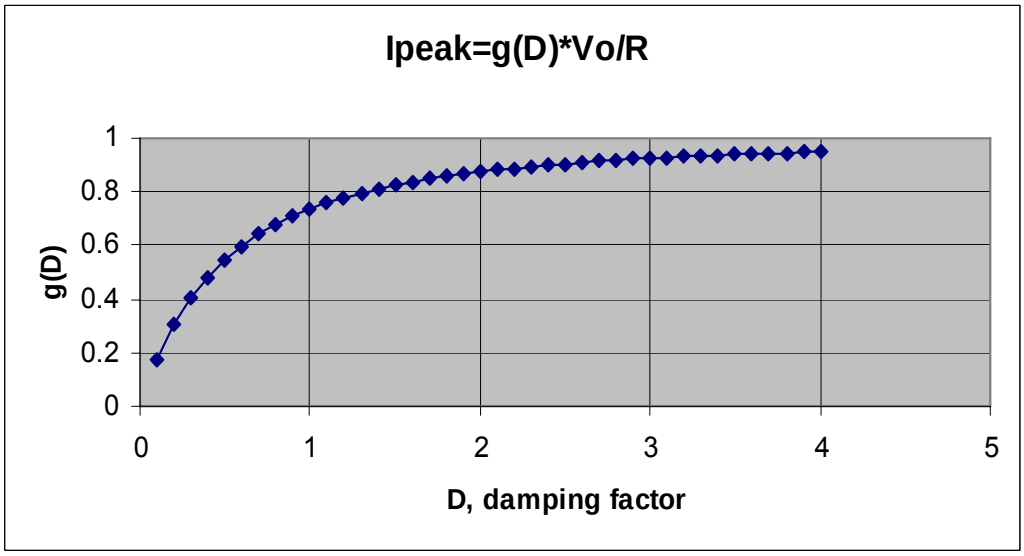

Figure A5. Plot of Eq. 9 showing how I_{peak} approaches V_0/R as a function of D.

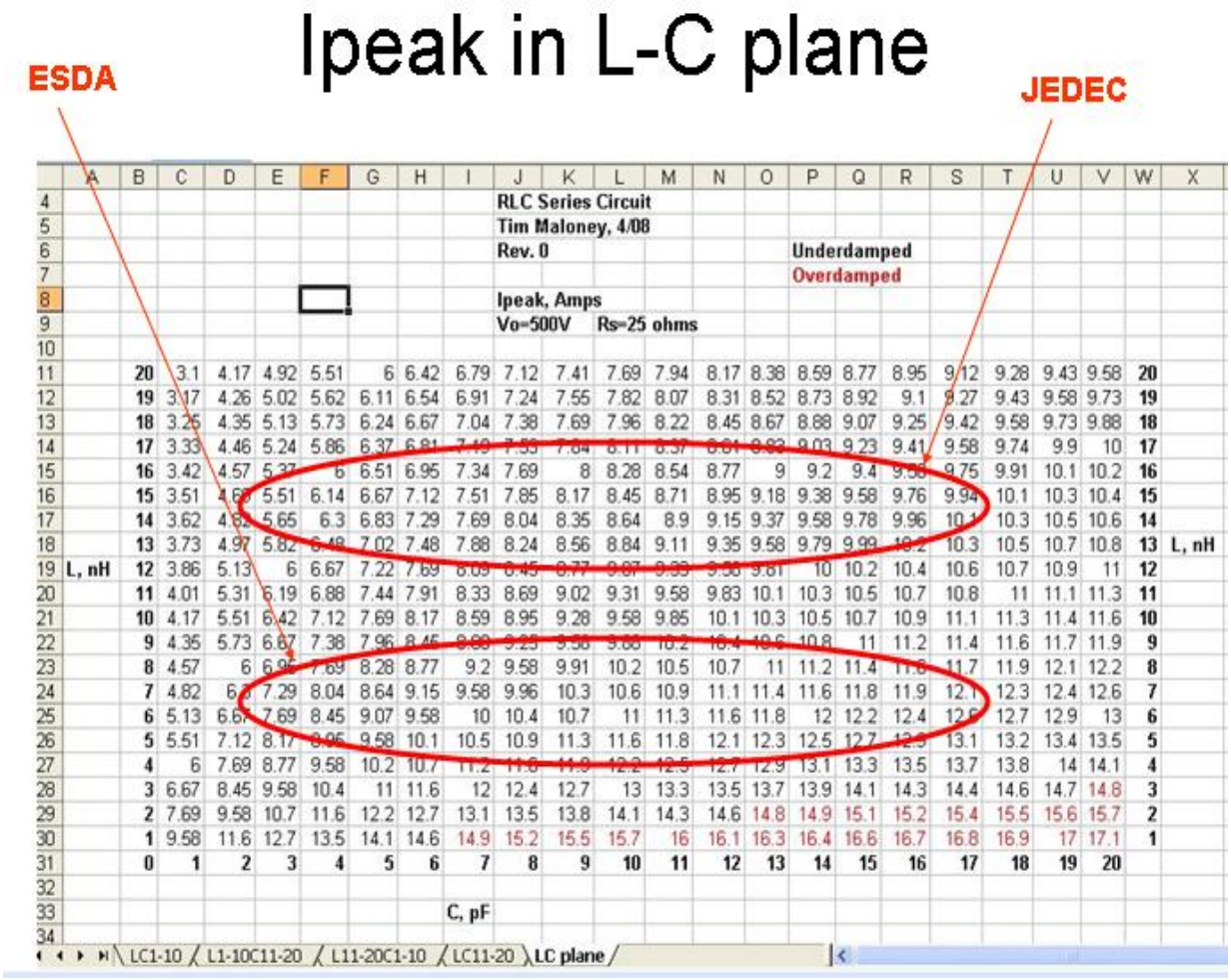

Figure A6: I_{peak} for simple series LCR discharge circuit, 500V, and typical values of L and C. R=25 ohms. Typical regions for the ESDA and JEDEC CDM testers are shown.

Figure A7 shows an example, from an Intel developmental test product, of a zap to Vss measured on a JEDEC CDM tester with a 1 GHz oscilloscope. The latter is low enough frequency to filter out any high-frequency effects that would give double peaks and such. The waveform looks to be underdamped, and the charge measurement from the integrated current gives a capacitance of 18-20 pF. Peak current is around 14 amps.

A best fit to these measurements then gives an equivalent spark resistance R of 38 ohms, as shown in Figure A8, another plot of I_{peak} in the L-C plane. This value of R is not unreasonable, particularly for a 2-pole model where we expect it to include the effects of intrinsic spark rise time, our would-be third pole in the analysis. As shown in Figure A8, the capacitance and peak current come out about as expected for the JEDEC CDM tester.

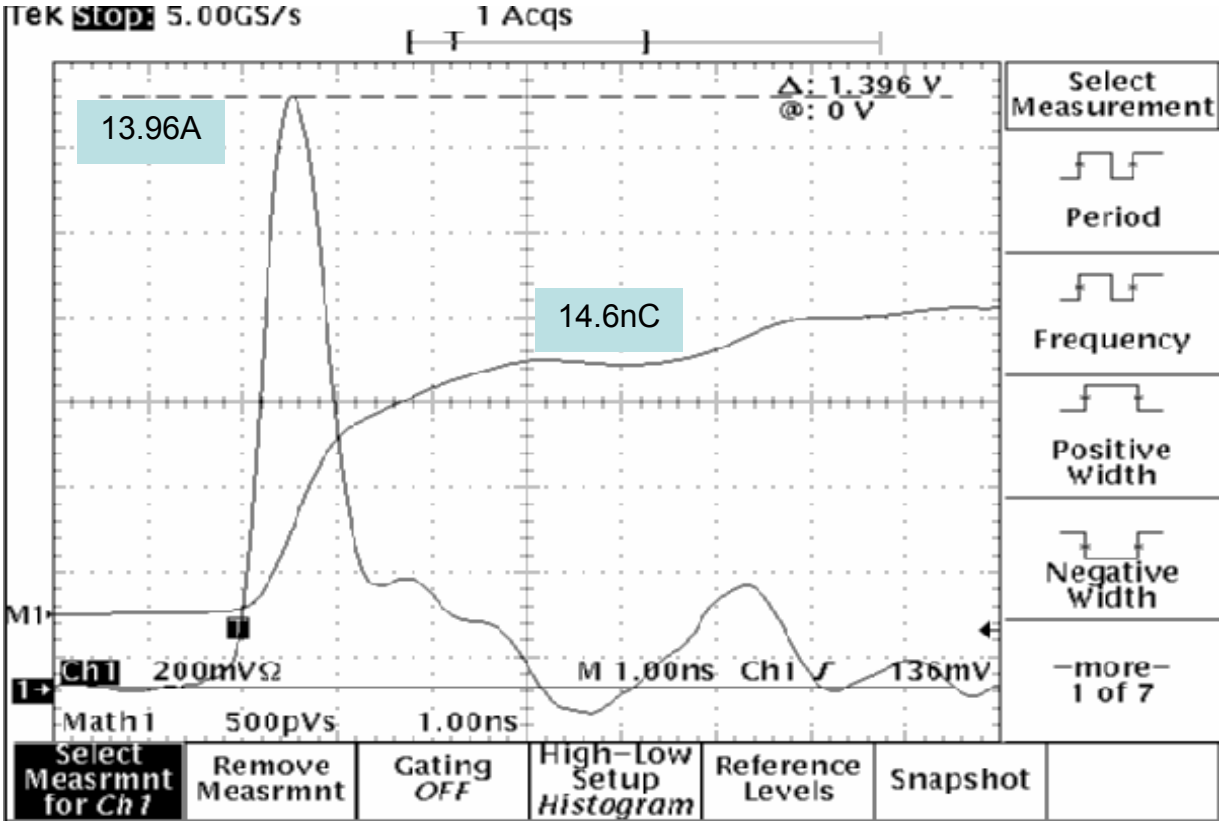

Figure A7: JEDEC CDM waveform at +800V on Vss plane of developmental product; peak current and total charge are shown.

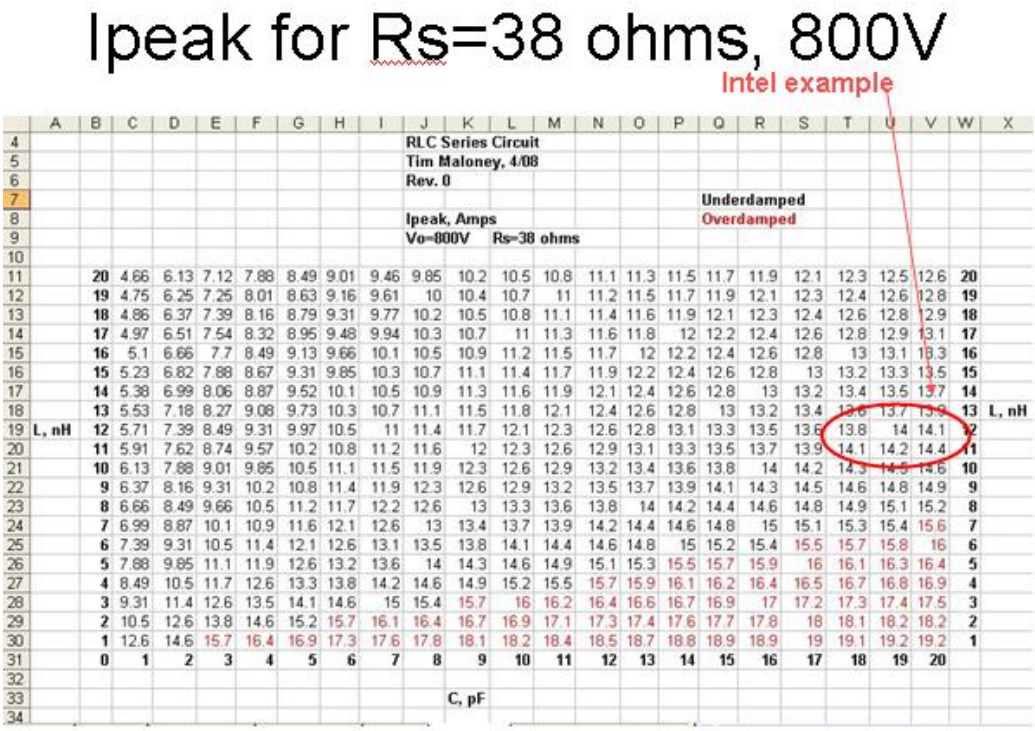

Figure A8: I_{peak} in L-C plane for series LCR discharge circuit, 800V, R=38 ohms. Location of Figure A7 example is shown, consistent with JEDEC CDM tester.

A.4 Conclusions

From the above analysis, it is clear that much can be understood about CDM testing of components from these relatively simple modeling considerations. A circuit model can focus on the primary lower-frequency effects and then be expanded to include higher-frequency effects if desired, using transmission line segments or appropriate approximations. The circuit models lead directly to solutions in the Laplace domain, which can convert to time-domain solutions through the inverse Laplace transform [8], or else be solved numerically using CAD tools like SPICE.

This kind of circuit modeling and related Laplace transform analysis can also be applied to two methods that have been used to achieve CDM-like pulsing on the wafer level, and as a substitute for ESDA or JEDEC CDM testing. One is the present author's wafer CDM (WCDM) technique [10], using a charged plate and probe above a grounded wafer and discharging at the pad. Please see Ref. 10 for much overlap with this appendix's analysis of ns-CDM, and further analysis in time and frequency domain of the WCDM method. The focus of WCDM is on simple overdamped solutions of the LCR circuit in order to achieve a CDM-like fast rise time and high peak current. The other method for CDM-like pulsing is capacitively-coupled transmission line pulsing (CC-TLP), which has been published for some time [11]. This method uses a step generator and 50 ohm line to force a pulse through a probe already connecting to a pad on the wafer. The ground return is through a grounded disk above the wafer (or grounded component) that forms the capacitive coupling. Spark resistance and rise time now resides in the TLP relay, although exclusive of any dispersion effects in the 50 ohm line. Also, spark resistance is remote from the 50-ohm line source and can be eliminated with attenuators or z-

matching. It is interesting to write an admittance function Y(s) for the CC-TLP case. Neglecting intrinsic or dispersed step function rise time, this would be

$$Y(s) = \frac{Cs}{LCs^2 + 50Cs + 1}, \quad (10)$$

very much like Eq. 3, except for the 50 ohm line impedance replacing the switch resistance. The inductance L is the very small inductance of the probe extending below the CC-TLP ground plate (there is some distributed probe capacitance too [12,13], but the probe impedance $Z=\sqrt{(L/Cp)}$ is fairly high), C is the ground plate cap. The waveform will be a double exponential (two real roots, overdamped) as long as $50 > \sqrt{(L/C)}$; very likely given a small probe inductance and a ground plate of reasonable size. The WCDM scheme [10] in its simplest form also has an admittance function resembling Eq. 10, where L can be a low probe inductance and an adjustable resistance is added to the arc resistance to replace the 50 ohms in (10) or R in (3).

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Appendix B: CDM Tester Limitations in Representing Real World Events

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B.1 Physics of Real World CDM

B.1.1 What is the physics of CDM? How does CDM occur in the factory?

CDM discharge of a device occurs if the potential difference between the charged device and an external metal object exceeds the breakdown voltage of the small air gap between them. The typical breakdown voltage of air is defined by the well known Paschen's curve. However real world events depend on a variety of conditions including the following:

-The discharge contact shape
-Capacitance, potential, and gap distance variability due to DUT motion
-Inductance variability due to package geometry and the geometry of the conductive discharge surface

If the charged voltage is roughly 2 kV or greater, a corona-like discharge can occur, which decreases the potential difference of the DUT before the CDM air discharge occurs. On the other hand, CDM testing requires good repeatability since it is a qualification tool in which capacitance, inductance, contact speed, environmental conditions, etc. are intended to be as constant as possible in order to meet the standard [1-4].

A basic CDM discharge is considered to be a rapid charge transfer between two objects as illustrated in Figure B1.

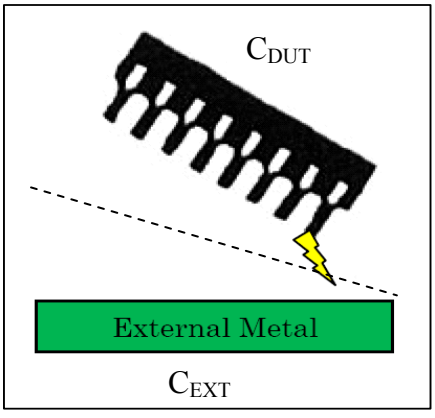

Figure B1: CDM Discharge between 2 objects. A single capacitance is partitioned into two series segments C_{DUT} and C_{EXT} as shown each with respect to a bisecting surface.

Figure B1 shows the discharge path between a DIP IC that has capacitance C_{DUT} and an external conductive surface with capacitance C_{EXT} (both with respect to a "reasonably drawn", but not rigorously defined, surface between them). Depending upon the environment, inductance and resistance may exist in the discharge path and will contribute to the voltage and current waveform discharge characteristics. When the dipole collapses and the potential difference is balanced between C_{DUT} and C_{EXT}, the discharge is complete.

B.1.2 Real World CDM Description of Device Potential / Charging / Discharge Mechanism

E-Field charging and tribocharging are the main methods of device charging:

E-Field charging: Changes in the electric field around a device change the potential of the device without changing the net charge on the device. The change in potential makes the device vulnerable to a rapid current pulse or CDM event when it contacts a conductor at a different potential. A charged person's sleeve nearing the device is an example of this type of charging.

Tribo-charging: Static charge is generated if a device slides on another surface. The generated charge depends on the materials of each surface, friction coefficient and the slide speed of the device. Several common examples exist in automated IC handling in manufacturing:

- **Devices sliding inside an IC shipping tube** is an example of this charging
- **Picking up from tape or a tray**: When a device is picked up from a device carrier, such as carrier tape or tray, charge is generated. This is a kind of tribo-charging.
- **Peeling off a sheet / tape and reel**. If a protection sheet is removed from the surface of electronic devices such as display device or CCD, the device is charged. This is also a kind of tribo-charging.

When a charged metal tool contacts a device, it causes CDM-like stress. This may be somewhat different from field induction or tribo charging; however it can be considered as a type of CDM stress, although the pulse width may be somewhat wider. This looks like System level stress depending on the size of the metal tool. Charged Board Events (CBE) may also be included in this category.

Advances in IC device and packaging technology have led to increased incidence of CDM events in modern manufacturing environment. In the early stage, IC packages were through-hole mounted and typically handled by machine or human hands. This has shifted to surface mount packages, with more automated machines being used. In mass production factories today, human handling is nearly nonexistent.

B.1.3 Early Stage Real World CDM Event Examples

Figure B2 illustrates an example where an IC package was charged by the friction between a marking roller and the package surface [5]. Another example was found in the IC tester where DIP packages slide in the tube followed by loading into the test socket.

Figure B3 is another example that illustrates 1) a corona discharge, followed by 2) a higher resistance air discharge, and then 3) a low resistance air spark discharge for an initial device charging voltage over 1000V [6]. The corona discharge reduces the device voltage before the air gap discharge is triggered. When the gap distance becomes smaller, a non-oscillation (higher spark resistance) discharge is detected, followed by an oscillation discharge (lower spark resistance) that is detected just before the contact. Spark resistance of the last discharge is less than 50 ohms, though 2nd spark resistance is typically over 100 ohms. If the contact speed is high enough, the second discharge is not typically detected. If the contact speed is too slow, more than two air discharges may occur until complete contact is made.

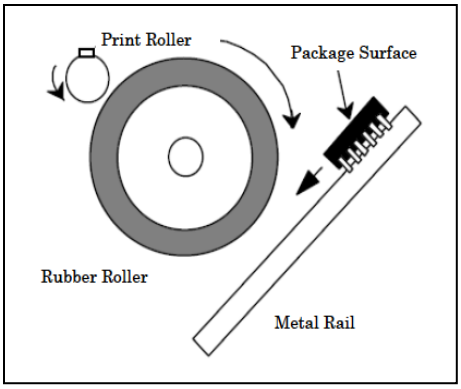

Figure B2: Early stage package Charging example

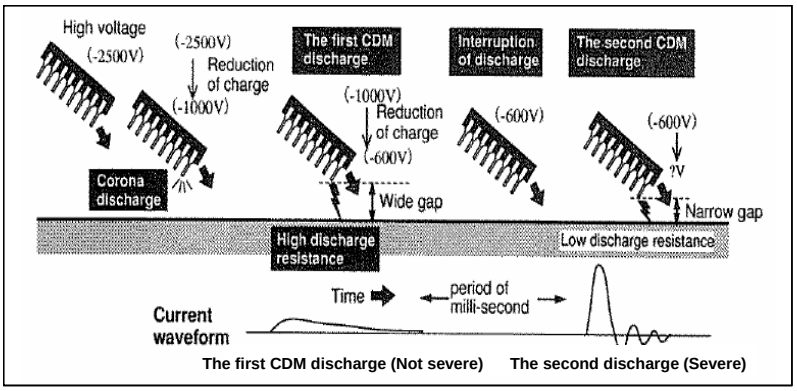

Figure B3: Example of multiple CDM discharge from High voltage devices

B.1.4 Recent Real World CDM Event Examples

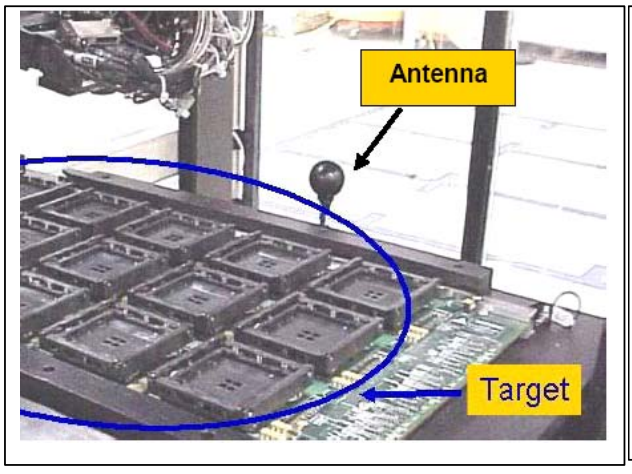

Figure B4: Advanced stage CDM example

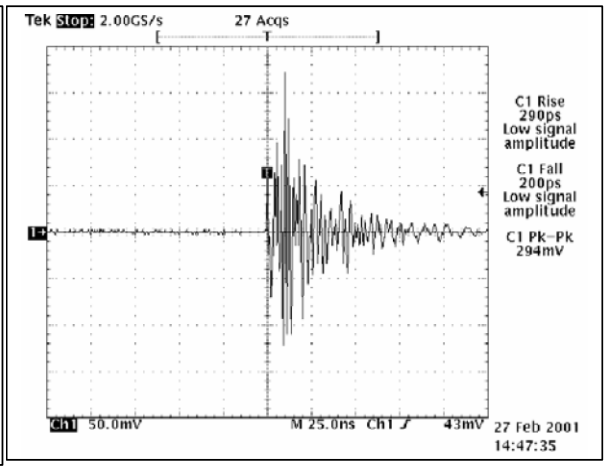

Figure B5: Scope waveform received by antenna shown in Figure B4

Since surface mount packaging is more common today, pick-and-place automatic machines are used everywhere in automated production lines. In this environment, more chance of field induced charging is found. Figure B4 shows an example where the device

is picked from a tray then loaded in the socket of a burn-in board. A CDM event happens if sufficient potential difference exists just before the contact between device pin and IC socket. The near field antenna in Figure B4 receives the electromagnetic field generated by this event and can be monitored by an oscilloscope as shown in Figure B5. It was reported that peak to peak voltage of this waveform is proportional to the CDM event charge if distance between the antenna and CDM discharge source is constant [7].

B.1.5 Capacitance Change Effect on Real World CDM Stress

Typical CDM discharges occur when any one pin of a charged integrated circuit approaches an external conductive surface. It is an air discharge that occurs just before the contact. Examples include:

Contact between IC and test socket
Contact between IC and PC board
Contact between IC and IC tray that has non-uniform resistivity

In the real world, handling is automated and capacitance between the handled device and a target object, such as a PC board where the device will be loaded, changes. The rate of capacitance change (increase) is highest just before the contact, in other words, just before the CDM event. Figure B6 is an example of the capacitance measurement that varies with the distance between a DIP devices and the ground plate [8]. Figure B6 shows that the capacitance of the device decreases down to roughly one tenth of the starting value as the distance increases to a few mm above the ground plate.

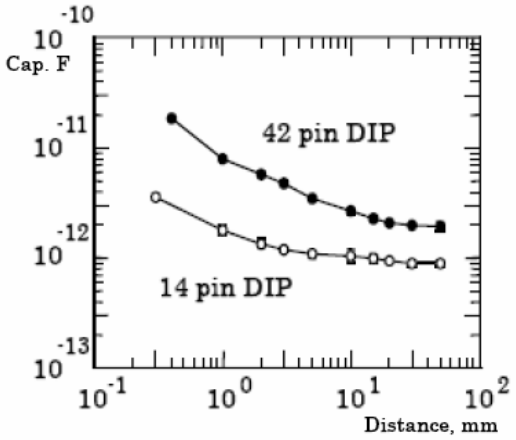

Figure B6: Device Capacitance vs. distance

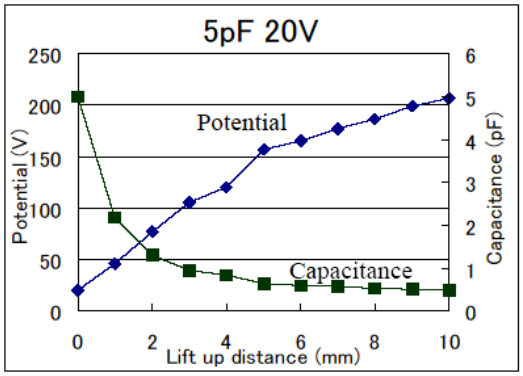

Figure B7: Device Capacitance vs. distance

This implies that if the amount of charge on the device is constant, the device potential decreases down to one tenth after approaching the ground plate from a distance of 10mm. This can also be illustrated by plotting discharge current versus the distance between the source of capacitance (i.e., the device) and the ground plate [9]. Figure B7 shows this relationship between distance and potential/capacitance. This graph shows that the potential of the capacitance module increased from less than 25V to over 200V by lifting up the device. Capacitance, on the other hand, decreased from over 5pF to less than

0.5pF. Since the peak current of the CDM event is proportional to the voltage across the gap, peak current decreases if the potential difference decreases due to the reducing gap distance. This reduces the CDM stress to the device. These phenomena are very common in real world CDM events.

B.1.6 Real World CDM Event Failure Types:

Figures B8 [10] and B9 represent examples of component CDM failures. Figure B8 illustrates gate oxide failure, a most common CDM failure mode. White spot at NMOS gate represents the emission site of failure in this picture. Figure B9 is another CDM failure example reported by Y. Fukuda, where a diode junction showed failure because diode diffusion spacing distance was not enough to limit breakdown.

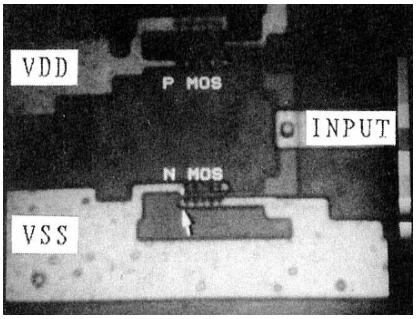

Figure B8: GOX Failure Example [10]

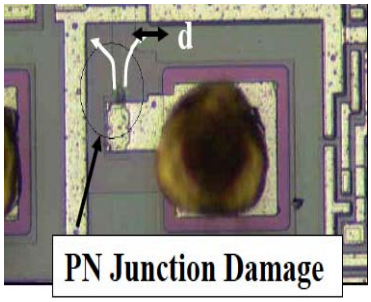

Figure B9: PN Junction Failure

B.2 Consideration and Analysis of Real World CDM

B.2.1 Circuit Model Representation of Real World CDM

Figure B1 can be described by the circuit schematic as shown in Figure B10. S represents the contact where the CDM discharge happens. R_{DUT} and L_{DUT} are series resistance and inductance in the DUT. L_{EXT} and R_{EXT} are inductance and resistance formed by the external conductive surface. Since all elements are serially connected, inductance and resistance values can be added together to create the simplified circuit model of Figure B11. R in Figure B11 includes R_{DUT}, R_{EXT} and the spark resistance of S. Sufficient voltage differential between V_{DUT} and V_{EXT} causes the discharge.

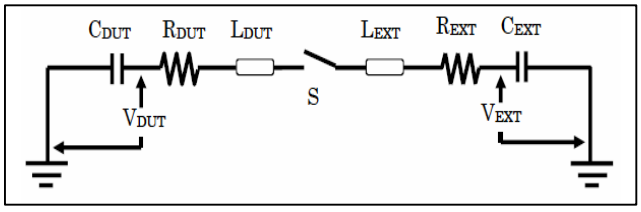

Figure B10: Real World CDM, Circuit Model

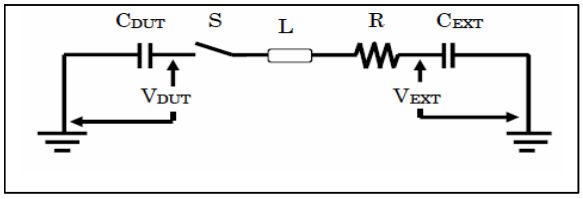

Figure B11: Simplified circuit of Figure B10

B.2.2 Real World CDM Stress Dependence on Package Style/ Size and Grounding

Because there are wide variations in factors affecting the real world CDM, it is difficult to compare every case. Typical cases are discussed here.

The CDM current is defined by the following equations [6] if the result of the portion of the equation inside of the square root is positive. V in this equation is the difference between V_{DUT} and V_{EXT} in Figures B10 and B11.

$$I(t) = \frac{V}{\omega L} e^{-\alpha t} \sin(\omega t) \quad , \text{ where } \alpha = R/2L \text{ and } \quad \omega = 2\pi f = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2} \qquad \text{Equations B.1}$$

On the other hand, the CDM Tester capacitance circuit model was reported as Figure B12 [7,12]. If this model is applied to the real world, Cfrg (plate to plate capacitance through the air) is usually much smaller than Cf (device to field plate through a thin dielectric). The series combination of Cfrg and Cf resembles C_{DUT} in Figures B10 & B11 while Cg resembles C_{EXT}; however they combine in parallel in the tester, not in series. As a result, the capacitance C in equations B.1 can be defined by the serial capacitance of C_{DUT} and C_{EXT} in Figures B10 & B11. For the tester, as described in Appendix A, Cg adds to the series combination of Cf and Cfrg. In both cases, a single equivalent capacitance results.

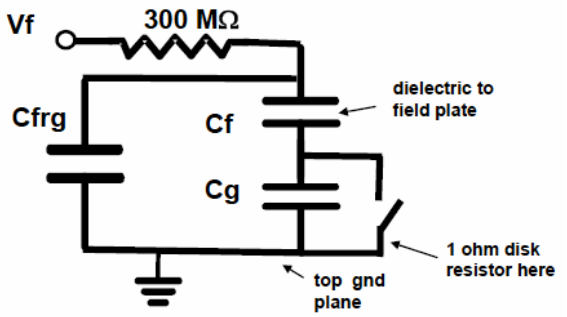

Figure B12: Capacitance model of F-CDM Tester

In Equations B.1 each parameter has following meaning in the real world:

V: Voltage difference across the gap just before the discharge (V_{DUT} - V_{EXT})
L: Inductance of the discharging path. This includes inductance inside the package such as bonding wire and lead length, and any external wiring such as the PC board pattern and the socket contact lead.
R: Series resistance of the discharge path. Arc resistance dominates real world CDM events and varies from about 10 ohms to above 100 ohms depending on the environment. Depending on the L and C values, the condition of the above equation ($R<2\sqrt{(L/C)}$) is not satisfied which gives a non-oscillating pulse (Figure B3 left).
C: Serial capacitance of C_{DUT} and C_{EXT} as described above.

Under the above assumptions, comparison between packages can be done as follows.

Between small package and large package (Small BGA and Large BGA)

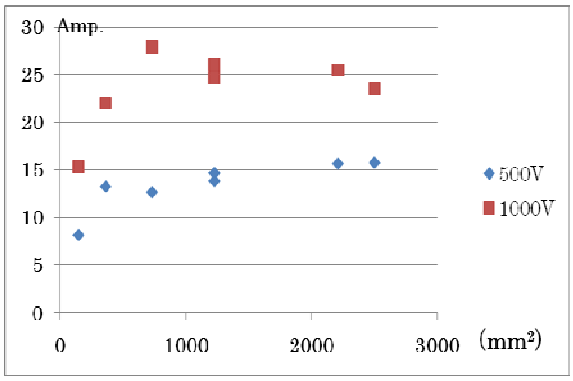

Figure B13: Peak current comparison between different BGA Package sizes

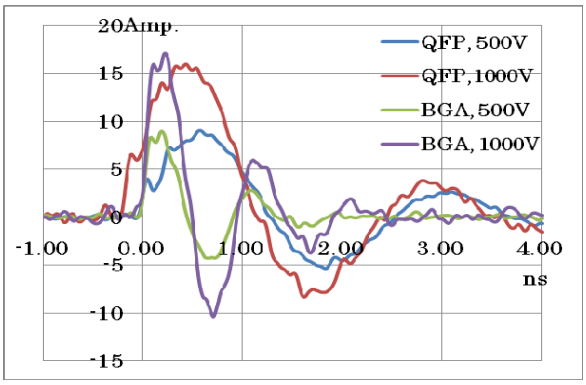

Figure B14: Peak current comparison between small BGA Package and large QFP both include same die

It is typical that a smaller package has a smaller C_{DUT} than a larger package. But it is the series combination of C_{EXT} and C_{DUT} that largely drives the peak current. C_{EXT} may be small, in the case of a small metal tool, and will drive the peak current accordingly. It is true in the tester world, too, where the equivalent C is defined by the standard [11]. Figure B13 shows a real world peak current comparison of a 12x12 BGA to a 50x50 BGA simulating the discharge to a small metal tool as shown in Figure B20. Because the tool C_{EXT} is typically much smaller than the device C_{DUT} in the real world (especially if C_{DUT} is high), current from a large package that has higher capacitance is almost constant. As shown in Figure B13, peak current increases only in the small capacitance region with package sizes less than 1000mm^2.

Between package types (BGA and QFP):

Figure B14 compares the waveforms from small BGA and large QFP packages containing the same die design. The package sizes of the BGA and QFP were 12x12 and 28x28 (mm^2 in both cases), respectively. The peak currents are equivalent, but the pulse width from the BGA is less than half of that from the QFP package. Note that these waveforms were measured using a 140mm x140mm top ground plate. It should be noted that the same current amplitude for the same die will not always be observed for different packages. A change in measurement conditions may result in a different current amplitude comparison. For example, if a lower bandwidth scope is used; actual peak current for the BGA package may be lower than for a QFP package due to the pulse width difference.

Through-hole type package and surface mount package:

Through-hole type packages are loaded on a PC board in such a way that IC leads connect through mounting holes on the PC board. In this method, the distance between the PC board and the IC body is greater than for a surface mount package where the IC lead tip contacts the PC board metal. This means that C_{DUT} of the through-hole package during a CDM event is smaller than C_{DUT} of the surface mount package. As a consequence, the voltage during the CDM discharge from a through-hole package is

higher than for a surface mount package, assuming that both packages hold the same amount of charge. However, discharging inductance L from a through-hole package is typically higher than that of a surface mount package. Bond wire length differences between these packages should also be considered for the current comparison. To compare the current difference from these package types, both V and C as well as L in equation B.1 should be considered.

Thickness of package (Surface mount packages):
In general, thinner packages have more C_{DUT} than thicker packages if the footprint is the same. If it is assumed that both packages begin at the same potential as they start moving far from the PC board, the eventual peak current from the thinner package is smaller than that from a thicker package because V is lower for the thinner package when the CDM event occurs.

Weight and package surface:
When sliding was the major consideration in device handling, weight and surface flatness were important parameters of charging. As surface mount packages requiring pick and place have become more commonplace, these parameters are not as important. Surface material and flatness may cause difference in charging. Mirror smooth surface packages have more chance of charging than coarse surface packages [10].

B.3 Differences Between Real World CDM and Tester World CDM

Table B-I: Comparison between Real World and Tester World CDM

Parameters	Real World	Tester World
Device capacitance (C_{DUT})	Depends on package and environment. Typically smaller than tester world	Stable, but depends on package, tester and test standard
Discharging capacitance (C_{EXT})	Depends on target object. Typically smaller than tester world.	Stable, but depends on package, tester and test standard
Capacitance between field plate and top ground (Cfrg)	Negligible in most cases	Determines equivalent C_{DUT}; can exceed real world
Charging voltage	Environment dependent.	Repeatable and definable
Discharging resistance	Depends on package, environment and contact material	Nearly stable, environment controllable
Discharging Inductance	Depends on package and target object	Constant, but depends on tester, test standard and device package
Peak Current	Depends on package and target object Lower than tester world in most case, especially on large package	Largely repeatable but dependent on package and Standards
Current rise time	From less than 100ps to a few ns	Stable but scope bandwidth limitation

Note: Table B-I compares CDM parameters between Real World and Tester World CDM. For Comparison between CDM standards, see Appendix C.

How is the real world represented by testers?

- The tester simulates the worst case of real world events.
- The tester provides a repeatable CDM evaluation.
- The tester stress level depends on the standard that tester complies with, such as JEDEC, ESDA, AEC or JEITA.
- If the current level of the real world CDM for the device is known, the same current can be applied to the device by the CDM tester. But all present CDM standards except ANSI/ESD STM5.3.1-1999 and ESD DS5.3.1-2007 use the low bandwidth (1GHz) scope that may not correlate to the real world current.
- Voltage or Current: Using only damage voltage does not well define the CDM ESD sensitivity since C (Capacitance) or I (current) is unknown.

B.4 CDM Waveform Comparison Between Real World and Tester

All CDM ESD Standards require that the commercial CDM tester conform to the current waveform specification [1-4]. Peak current discharged from small and large verification (capacitance) modules should fall within the ranges of Table B-II. Capacitance values of the small and large module in JEITA may be different (about 15% less) from what is listed in Table B-II since the JEITA standard recommends a nominal 4.0 dielectric constant insulator sheet above the ground plate (although the coin modules are very close to the JEDEC standard). These standards also specify current pulse rise time and width. Since the verification modules do not include any inductance, only tester inductance is included in the discharge path.

Table B-II: Peak Current Comparison Table Between CDM Standards.

	JEDEC[1]	ESDA[2]	AEC[3]	JEITA[4]
Small	5.75A(±15%) at 500V	7.5A(±20%) at 500V	4.5A(±20%) at 500V	4.0A(±10%) at 500V
Large	11.5A(±15%) at 500V	18A(±20%) at 500V	14A(±20%) at 500V	5.5A(±10%) at 500V
Notes	Scope: Min.1GHz BW Small:6.8pF±5% Large:55pF±5%	Scope: Min. 3.5GHz BW Small:4pF±5% Large:30pF±5%	Scope: Min. 1GHz BW Small:4pF±5% Large:30pF±5%	Scope: Min. 2GHz BW

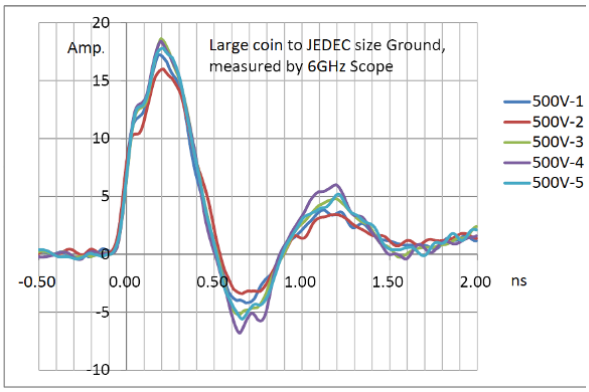

Figure B15: Large Coin to JEDEC size ground

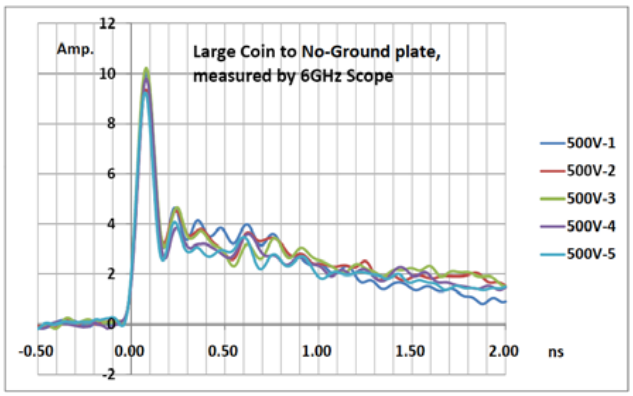

Figure B16: Large Coin to no top ground plane

Figure B15 shows current waveform measurements from a large JEDEC verification module to a JEDEC size ground (63.5mm x 63.5mm) at a charge voltage of 500V. Figure B16 shows the current waveform from the same large coin module without a top ground plane. The current waveform is very different between these figures. The current for the JEDEC size ground plate is 50 to 80% higher than the current for a module without a top ground plane. While the waveform of the module with a ground plate is a damped oscillation, the waveform of the module without a ground plane shows a short single pulse. Figure B16 is closer to the real world CDM event waveform than Figure B15 since the top ground plane in a real world CDM event is not usually as large as for CDM in the tester world.

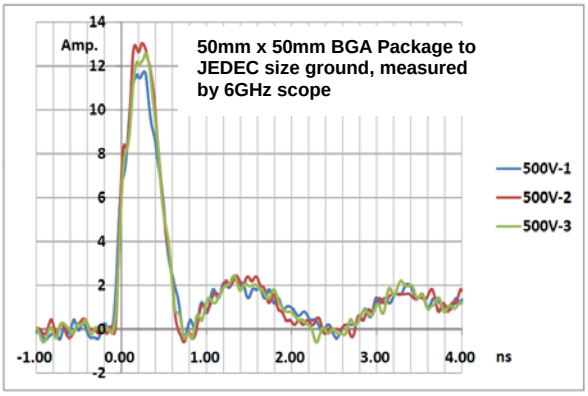

Figure B17: Large BGA Package to JEDEC size ground

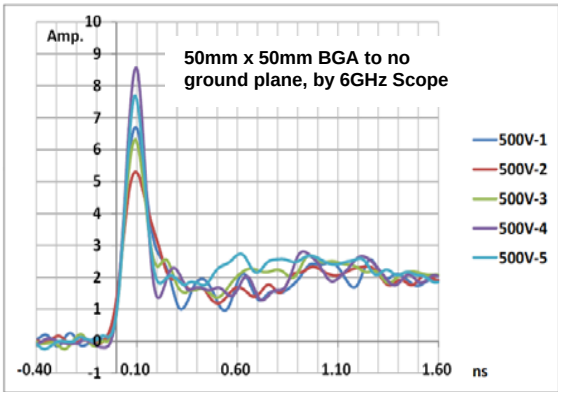

Figure B18: Large BGA Package to no top ground plane

Figure B17 shows the current waveform discharged from a 50mm x 50mm BGA package device to a JEDEC size ground plate with a charge voltage of 500V. If the ground plate is removed, the waveform in Figure B18 results. The relationship between Figures B17 and B18 is very similar to the relationship between Figures B15 and B16. If the ground plate is removed, the discharge current does not oscillate and the pulse width is very short compared to the waveform with a ground plate. The capacitance of this BGA package when placed on a 0.4mm thickness JEDEC insulator was about 100pF.

Figure B19 illustrates the discharge path inductance effect on peak discharge current for a small coin, a large coin, a small BGA and a large BGA at 500V. The top ground was a JEDEC size plane. Contact rod lengths of 2mm, 5mm and 10mm were used. Figure B19 indicates that the peak current decreased to roughly 1/2 with a contact rod length increase from 2mm to 10mm for the large capacitance devices. Peak current from smaller capacitance devices are not affected as strongly as higher capacitance devices.

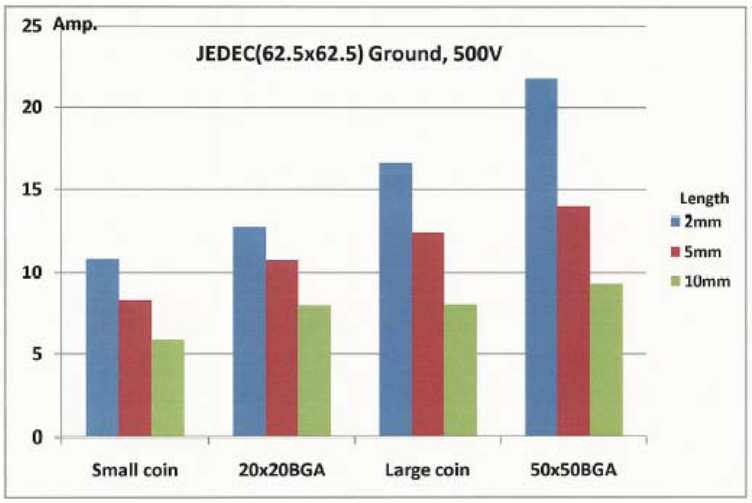

Figure B19: Contact Rod Length Effect to Peak Current of Devices

In real world CDM environments, the discharge "ground" does not resemble a large ground plane as in the worst case tester environment. This means that the peak current of the real world CDM event is not as high as the tester world. The current probe used in the above experiment is shown in Figure B20.

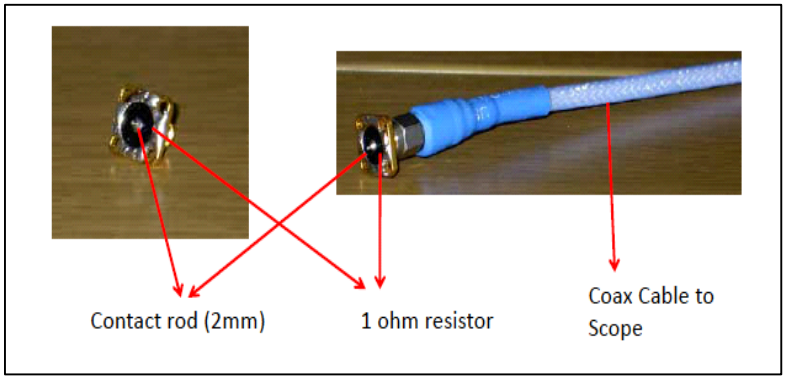

Figure B20: Current probe used in the above experiment: Different size top ground plane was mounted by the 4 holes on the connector corners

B.5 Conclusions

Real world CDM events were evaluated and compared to the tester world, with the following conclusions:

- Real World CDM events are not as repeatable as a tester world CDM discharge.
- Discharge current from higher capacitance devices increases if the top ground size in the tester world is larger.
- In real world CDM events, a very low inductance discharge to a large upper ground is extremely rare. Since the serial inductance of a real world CDM event is typically higher than in the tester world, the peak current is not as high as in the tester world. If a 10mm wire (roughly 13nH) exists in the discharge path, the peak current from higher capacitance device will be 50% less than if a 2mm wire discharge were used. (Figure B20)
- Charged Board Events (CBE) is not included in this discussion of real world CDM events. CBE should be handled separately and is discussed in Appendix E.

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Appendix C: CDM Qualification and Test Methods

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Robert Ashton, ON Semiconductor
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This appendix summarizes existing CDM ESD test methods and standards and differences between them, and demonstrates the impact of the differences on product test results. It explains the weaknesses of the existing test equipment and methods that lead to inconsistencies and non-repeatability issues in product test results. This appendix demonstrates that these deficiencies are in part attributable to missing specifications in the standard test methods, such as the size of charge plate or the ground plane, which results in a strong dependency of test results on the tester manufacturer, type and setup parameters. It will show that reproducibility and non-repeatability issues are also due to fundamental properties of the currently widely used air discharge test method. This appendix will also demonstrate that the current CDM voltage classification levels apply more stress to larger and thinner devices than to smaller and thicker devices for the same classification level.

C.1 CDM ESD Testing Methods

All ESD events are governed by two fundamental properties, a capacitor that becomes charged and a current discharge path. CDM testing is unique from other ESD tests in that the capacitor is dominated by the properties of the IC device being tested and not by an external capacitor, as for example in the HBM ESD test [1][2] The capacitance relevant for CDM is the capacitance of the device under test to its surroundings, typically a nearby ground plane. During CDM ESD events, the chip and package impedances also significantly influence the discharge current path.

A CDM standard test method must address the following issues:

1. Produce a capacitance that scales with the IC's size and reproduces the IC device's capacitance to its surrounding during a real-life event.
2. Provide a method to rapidly transfer charge to or from this capacitance through each individual pin of the IC device while:
    a. Creating a reproducible discharge event.
    b. Maintaining a low impedance path for the discharge current.
    c. Ensure that a discharge event has occurred.
    d. Accurately measure the discharge current.

C.1.1 Non-Socketed CDM ESD Test Methods

For non-socketed CDM ESD tests, the device under test (DUT) is placed in a "Dead Bug" or "pins up" position, on top of a metal plate as shown in Figure C1. This creates a capacitance between the DUT and its surroundings that depends on the size of the DUT. Depending on the specific standard and test method applied, an insulator may be placed between the DUT and the metal plate. The presence, type and thickness of this insulator vary between the test standards.

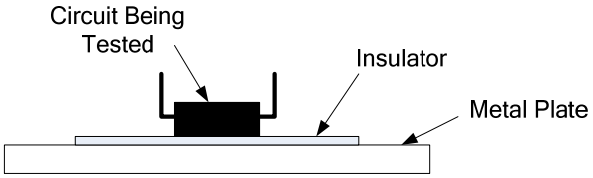

Figure C1: Capacitor formed by placing IC on top of metal plate.

A. Charging Method

Two different charging methods, "direct" and "field induced" can be used to charge the IC device's capacitance as illustrated in Figure C2. In the direct charging method, contact is made with a robotic probe to one pin of the IC device, often a substrate connection. The electrical potential of the IC device is elevated to a high voltage level by connecting a high voltage supply to this pin through a high value resistor, usually many megohms.
For the field induced CDM charging method, a metallic ground plane is placed over the IC device and the metal plate, which is called the field plate when this charging method is applied. The electrical potential of the field plate can be controlled with a high voltage power supply through a high value resistor. If the capacitance between the field plate and the IC device is much higher than the capacitance between the IC and the ground plane, the electrical potential of the IC device will closely follow the electrical potential of the field plate. The net result of raising the voltage level on the field plate is to raise the electrical potential of the IC device relative to the ground plane above it. Unlike the direct charging method, the field induced method does not transfer charge to the device under test during this "charging step".

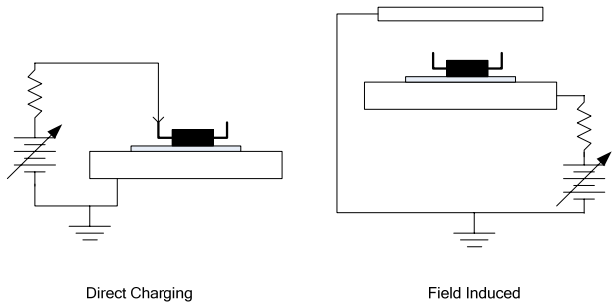

Figure C2: Direct charging and field induced charging method.

B. Discharge Event

Discharge of a directly charged IC device can occur in one of two ways, as illustrated in Figure C3. A grounding electrode may make contact with the pin under test, by creating an air discharge, or the pin may be discharged through a relay. In some cases the same electrode is used to charge and discharge the IC device as is illustrated in Figure C3.

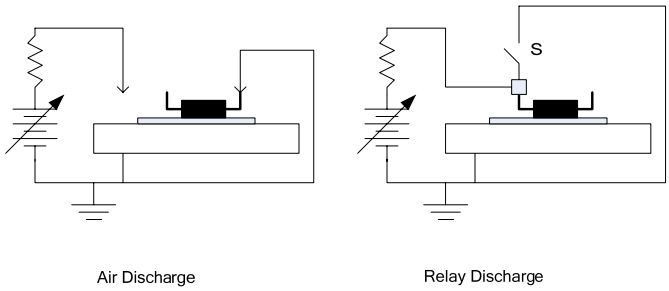

Figure C3: Discharging of a directly charged IC.

In the field induced method the stress event is more properly defined as a grounding of the device under test than a discharge, since the IC device actually becomes charged when it is grounded. This method is illustrated in Figure C4. In the center of the ground plane is a spring-loaded pin, commonly called a pogo pin. The pin is in the center of a circular 1Ω resistor.

As the pogo pin approaches the IC device's pin under test, high electric fields occur between the two electrodes. When a critical electric field strength is reached, the air will breakdown and an arc will form between the grounded pogo pin and the IC device's pin. A charge transfer will now abruptly occur to ground through the pogo pin. The discharge event results in a net charge on the IC device as the grounding of the pin actually charges up the IC device.

As the discharge current flows through the pogo pin and circular 1Ω resistor, the discharge current can be measured as a voltage drop across the resistor and can be recorded either by an oscilloscope or a pulse detection circuit.

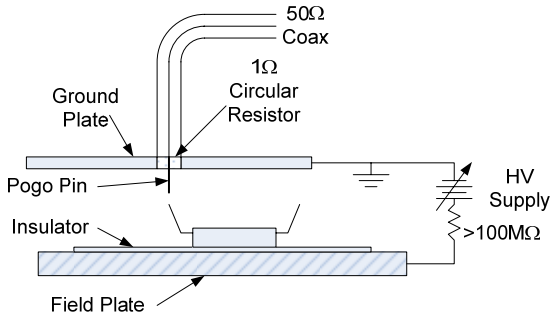

Figure C4: Field induced CDM.

C.1.2 Socketed CDM ESD Test (SDM)

The ESD Association's (ESDA) Socketed Device Model (SDM) [3] was developed as a way to perform CDM testing using a relay matrix based automated HBM tester. In this Standard Practice test method the IC device is placed in a socket on the ESD tester and is charged to a high voltage level, typically through all ground pins or through all pins in the device. For the pin under test, a relay is closed and the charge stored in the IC device and in the parasitic capacitive elements inside ESD tester is discharged. This method has been successfully used by several companies to identify "CDM like" circuit weaknesses and to replicate field failures.

However, since the background tester capacitance for this test method is approximately 25 – 30 pF, the discharge in this method is dominated by the capacitance in the ESD tester more than by the capacitance of the IC device. Since this test method is quite different from either field induced or direct charge "CDM only" test methods, comparing

test results and fail voltages is difficult. Due to these described drawbacks, this method is not widely used and will not be further discussed.

C.1.3 Small Capacitance Model

In Japan a small capacitance method has been developed and documented by JEITA. In this method a small capacitor (≤ 10pF) is formed within the same assembly as a low inductance switch. The capacitor is charged and discharged into one pin of an IC while another pin is grounded. This model is used only by a few companies in Japan. Due to its limited relevance, it will not be further discussed.

C.1.4 Capacitive Coupled Transmission Line Pulsing (cc-TLP)

Capacitive Coupled Transmission Line Pulsing (cc-TLP) [4][5] is an alternative method to generate CDM-like stress on devices and reproduce the electrical and physical failure signatures of CDM ESD events. The cc-TLP test system injects a rapid rising narrow high-current pulse, which is well-reproducible, into a single stress pin of a device after an electrical contact is established to this pin. The exponentially decaying charging current (RC) distributes over the full device like FCDM testing and generates voltage drops internal to the device. While this test method is currently already used to determine the robustness of products at wafer level and for CDM failure debugging, this method is currently not applicable for qualification purposes.

C.2 Comparison of Existing CDM Standards

C.2.1 Comparison of Standard Documents

A. Comparison of Key Parameters

There are 4 primary standards for CDM:

- JEDEC JESD22-C101D [6]
- ESDA ANSI/ESD STM5.3.1-1999 [7]
- AEC AEC-Q100-011 Rev-B [8]
- JEITA EIAJ ED-4701/300-2 Test Method 305 [9]

The key parameters of these standards are compared in Table C-I. The JEDEC and AEC/ESDA standards are the most commonly used standards, while the JEITA standard is mostly used in Japan.

Table C-I: Comparison of key CDM features of different standards.

Organization	**JEDEC**	**ESDA**	**AEC**	**JEITA**
Standard	JESD22-C101D	ANSI/ESD STM5.3.1-1999	AEC - Q100-011 Rev-B	EIAJ ED-4701/300-2
Charging Method	Field Induced	Field or Direct	Field or Direct	Direct or Field
Calibration Modules	Metal Coins	Metal Film on 0.8mm FR-4	Metal Film on 0.8mm FR-4	Metal Film on insulating sheet
Insulator Thickness (mm)	0.381 ± 0.038	none to ≤ 0.13	none to ≤ 0.13	0.40 ± 0.04
Insulator Dielectric Constant	4.7 ± 5%	Not Specified	Not Specified	4.0 ± 0.5
Discharge	Air	Air	Air or Relay	Air or Relay
Current measured during CDM stress	Yes	Yes	Yes	Not required
Number of Discharges + & -	3	3	3	1
Number of Parts	3	3	3	Not specified
Calibration Voltage Levels	200, 500, 1000	125, 250, 500, 1000, 1500, 2000	250, 500, 1000, 2000	500, 1000

B. Comparison of Waveform Parameters

Table C-II: Comparison of CDM current waveform properties for different standards (JEDEC, ESDA, AEC & JEITA) at 500V: peak currents, rise times and full width at half height (FWHH).

Standard (Scope bandwidth)	**Small Module**				**Large Module**			
	C [pF]	**I_{peak} [A]**	**t_{rise} [ps]**	**FWHH [ns]**	**C [pF]**	**I_{peak} [A]**	**trise [ps]**	**FWHH [ns]**
JEDEC (1GHz)	6.8	5.75 ± 15%	<400	1±0.5	55	11.5 ± 15%	n/a	n/a
ESDA (3.5GHz)	4	7.5 ± 20%	<200	<0.4	30	18 ± 20%	<250	<0.7
AEC/ESDA (1GHz)	4	4.5 ± 20%	<400	<0.6	30	14 ± 20%	<400	<1.0
JEITA (≥2GHz)*	~6.8**	4 ± 10%	≤300	≤0.6	~55**	5.5 ± 10%	≤400	≤0.8

* JEITA peak current values for the standard verification method. There is an alternative method specified in the standard that has different peak current values.

** JEITA specified the diameter of the coin used for the verification, not the actual capacitance. The size is comparable to the values defined in the JEDEC specification.

Table C-I and Table C-II demonstrate that there are many differences between these standards that make CDM test results difficult to compare. It is generally true though that the most critical CDM waveform parameter that leads to IC device failures is the peak current, I_{peak}. A comparison of I_{peak} values is shown in Figure C5. Rise time can also be important depending on the turn on time of protection circuitry and the full width at half height can relate to the total energy deposited into the device being tested.

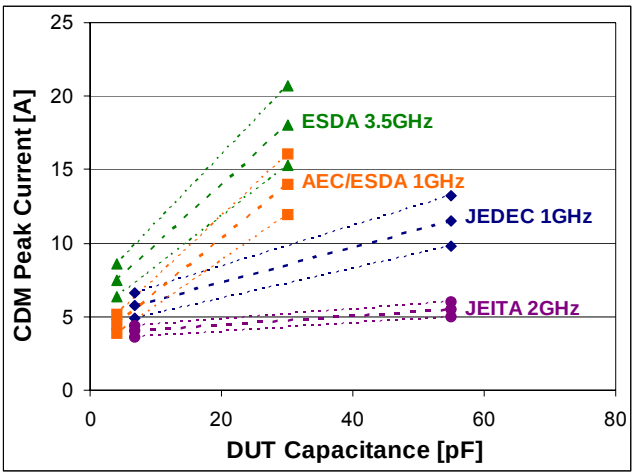

Figure C5: Differences in expected CDM peak currents for different standards depending on the capacitance of the verification module. Some of the differences are due to specifications of the peak current for oscilloscopes with different bandwidth limits.

C. Thickness of Insulator on Field Plane

One of the main differences that directly affects the peak current is the insulator thickness on the field charging plate. The ESDA and AEC standards specify at most a 0.13 mm thick insulator but also allow a field plate with no dielectric. JEDEC uses a 0.381 mm insulator while the JEITA standard calls for a 0.4 mm insulator. Therefore, the device capacitance will be different for each standard. Any significant changes to the package thickness will cause more of a change in the capacitance in the ESDA and AEC standards than in the JEDEC or JEITA standards.

D. Accuracy of Verification Modules

Each standard specifies a calibration module to be used for waveform calibration and verification. In Table C-II the specifications for this module are quite different between the two major test methods, JEDEC22-C101D and ANSI/ESDA STM5.3.1-1999. The JEDEC modules are coin shaped disks, which are placed on the 0.381 insulator that is part of the JEDEC setup, while the ESDA uses a metal film on top of a 0.8 mm thick sheet of an FR-4 circuit board as a calibration module. This fundamental design difference directly affects the value of the peak currents that are measured. These two issues imply that when comparing CDM test results between different standards a simple scaling ratio will not be valid.

E. Oscilloscope Bandwidth

Another area, where the measurement accuracy of I_{peak} can cause unwanted variations, is the difference in the oscilloscope bandwidth requirements in the standards. When the CDM standards were first written, the cost of a high bandwidth oscilloscope that measured in the gigahertz frequency range was extremely expensive. As a consequence, the bandwidth required for the oscilloscope used for the verification was relatively low. Today, the costs for this type of test equipment have decreased dramatically, but the oscilloscope specifications have not changed. Table C-II shows the test equipment requirements for the different CDM standards. JEDEC and AEC only call for 1GHz oscilloscopes. JEITA requires an oscilloscope with a bandwidth of 2GHz or more. ESDA

allows for oscilloscopes with two different bandwidths, 1GHz and 3.5GHz. Measurements at 1GHz are quite marginal for the speed of CDM events and recent reports indicate that there can be considerable differences in waveforms when viewed with oscilloscopes with bandwidths greater than 3.5GHz [10]. This variation in measurement bandwidth makes it more likely that discharge current waveforms may have much more variability than the standards waveform specification values imply. These differences in oscilloscope bandwidth requirements in the standards make the comparison between the standards even more difficult.

F. Size of Ground Plane

The different standard test methods are inconsistent in their specifications and not sufficient for today's packages. The ESDA method requires that the ground plane must completely cover the IC device, while the JEDEC method specifies a fixed size of 63.5 +/- 6.35 mm for this setup parameter. When the CDM standard was first developed in the late 1980s and early 1990s, the largest IC device package capacitance was less than 30 pF. Hence, the specified requirements were more or less adequate as the dependence of peak current on device size is a linear function for small capacitive values ranging from 0 to 40 pF. Today, very large IC packages with capacitance in the nanofarads are becoming more commonplace. The introduction of these large packages has resulted in hardware configuration problems where the ground plane cannot completely cover the package. Hence, the dependence of peak current on device capacitance saturates at capacitance values greater than 40 pF [16]. As a consequence, the test results for these large devices can vary significantly, depending on the size of a ground plane used on a particular tester and can vary even more significantly between different tester types and configurations. This hardware problem makes CDM testing difficult and obtaining repeatable results challenging.

G. Air versus Contact Discharge

The difference in the discharge current waveform between air discharge and discharge in a relay can be significant. In the simplest 2-pin configuration, relay switch discharges are expected to be more consistent, but the added inductance of the relay will increase pulse rise time, reduce peak current at a given CDM voltage, and increase ringing. Any attempt to convert the 2-pin configuration into a relay matrix network will introduce unwanted tester RLC parasitics and change the fundamental properties of the CDM discharge current waveform.

H. Summary

This comparison of the existing CDM test standards highlights significant differences in the tester setup parameter specification and actual current waveform measurements methods. These differences are significant enough that a product CDM fail voltage level would be unique to that test method. Applying a simple scaling ratio to calculate the failure level between the standards would not produce consistent and correct results.

C.2.2 Product CDM Test Correlation Data

This section summarizes results from several experiments that tested IC devices using the primarily used and Industry accepted CDM testing standards ESDA, JEDEC, AEC and

JEITA. The results from these experiments demonstrate that the differences in the standards lead to differences in the CDM ESD product pass and fail voltages.

Example 1

A CDM ESD correlation study [12] was performed to compare CDM failure levels for the same IC devices between ESDA and JEDEC standards. All devices were tested according to the JESD22-C101D and ANSI/ESDA STM 5.3.1 standards. CDM discharge current waveforms using the verification module for each standard showed, as expected, higher peak currents for the ESDA standard compared to the JEDEC standards for the same voltage level. Consequently, CDM test results shown in Table C-III failed at lower stress voltage levels for the ESDA compared to the JEDEC standard.

Table C-III: ESDA versus JEDEC Correlation Test Results

CDM Stress Voltage	ESDA failing / tested units	JEDEC failing/tested units
250V	0 / 3	0 / 3
500V	2 / 3	0 / 3
750V	-	3 / 3
1000V	3 / 3	3 / 3

Example 2

A similar CDM ESD correlation study [13] compares CDM failure levels between ESDA and JEDEC standards for the same IC device. The CDM test results highlighted in Table C-IV show failure at lower stress voltage levels for the ESDA standard compared to the JEDEC standard. The devices were stressed at 25V or 50V increments. The largest difference observed in this study was more than 400V or 100%.

Table C-IV: JEDEC versus ESDA Correlation Test Results

CDM Withstand Voltage [V]			
Part	**Pin Type**	**JEDEC**	**ESDA**
A	**1**	**800**	**550**
A	**2**	**850**	**600+**
A	**3**	**800**	**500**
A	**Part**	**800**	**500**
B	**Part**	**800+**	**400**
C	**Part**	**550**	**350**

Notes:

- "+" means passed the highest voltage tested
- "Part" means level for entire part (all pins tested)
- These are not necessarily shipped products; they may have been for evaluation only

Example 3

In another CDM ESD correlation study [14], JEDEC's Field Induced Method and JEITA's Direct Charging Method were directly compared. In addition, the research also studied the CDM fail voltages between die assembled in two different package configurations. The Device A was built in a 65 nm bulk CMOS technology and the die was assembled in both a BGA and QFP package configurations. Device B was built in a 65 nm bulk CMOS technology and Device C was built in a 90 nm bulk CMOS technology. Both were assembled in BGA package configuration.

The test results summarized in Table C-V showed significantly lower CDM fail voltage levels for JEDEC compared to JEITA standards. These test results were expected since the peak current levels during calibration for the JEITA standard are much lower than those for the JEDEC standard. The devices fail at approximately the same current levels for both standards (see Figure C6).

Table C-V: JEDEC versus JEITA Correlation Test Results

	JEDEC Field Ind. Charging CDM Voltage [V]	**JEITA Direct Charging CDM Voltage [V]**
Device-A (BGA 1212)	900	1300
Device-A (QFP 2828)	900	1300
Device-B (BGA 1515)	800	1400
Device C (BGA 3333)	600	1200

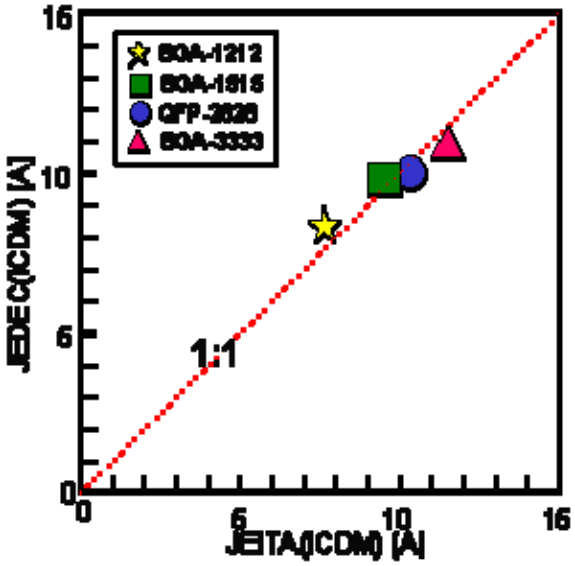

Figure C6: Correlation of the CDM Fail Current Levels between JEDEC Field Induced Method and JEITA Direct Charging Method.

Example 4

In a comprehensive correlation study [15], a special small scale circuit was evaluated for CDM robustness. The device was built in a 90 nm CMOS process and assembled in a PBGA388-2727-1.0 package. The purpose of the correlation study was to compare CDM failure levels for the same IC devices between ESDA, JEDEC and JEITA CDM standards. The research also compared three different types of SCR ESD protection circuit listed as Device A, Device B and Device C. The test results showed the lowest CDM voltage level for ESDA, a somewhat higher level for JEDEC and at the highest level for JEITA. This trend was expected and correlates with the expected peak currents for the respective standard. All three test method generated the same CDM gate oxide failure mechanism. The results of this study are summarized in Table C-VI.

Table C-VI: ESDA, JEDEC versus JEITA Correlation Test Results

	ESDA Direct Charging CDM Voltage [V]	**JEDEC Field Ind. Charging CDM Voltage [V]**	**JEITA Direct Charging CDM Voltage [V]**
Device-A	**750**	**1100**	**1600**
Device-B	**400**	**600**	**900**
Device-C	**300**	**450**	**650**

The results from the studies presented in this section confirm also that no simple scaling rules that can be used to relate test results from one standard to another. This is mainly due to the differences in the test fixtures for the different standards.

C.2.3 Conclusions

Different CDM testing standards will produce significantly different CDM voltage withstand levels for the same device. The results from one standard cannot be transferred to another standard by applying a simple scaling rule as this would most likely produce incorrect results.

C.3 Weaknesses of Existing Test Methods and Standards

Today's CDM test standards do not completely define all of the critical setup parameters required to achieve "repeatable" discharge waveforms between different simulators. Consequently, product pass and fail voltages can vary widely between different CDM simulators, even when the same standard is applied.

C.3.1 Inadequate Specification of CDM Test Equipment

The existing CDM ESD test standards include a minimum amount of detailed information about the required properties of a CDM tester. Examples for values that are included in some standards [6][7][8][9] are summarized in Table C-VII. The remaining dimensions and parameters, such as the size of the ground plane and charging plate, the length of the pogo pin, and the inductive and capacitive parasitics in the discharge path, are only implicitly defined. These parameters have to be sized such that the waveforms resulting from a CDM discharge on the verification modules meet the respective waveform requirements defined in the standards. These parameters are: peak current, rise time, full width at half height, undershoot, and overshoot (for values see Table C-II).

Table C-VII: Definite CDM Tester Requirements Included in Different Standards.

Organization	JEDEC	ESDA	AEC	JEITA
Standard	JESD22-C101D	ANSI/ESDA STM 5.3.1	AEC - Q100-011 Rev-B	EIAJ ED-4701/300
ground plane size	63.5±6.35mm	**not specified**	**not specified**	**not specified**
dielectric thickness	0.381±0.038mm	≤0.13mm	≤0.13mm	0.4±0.04mm
dielectric constant	4.7 ± 5%	not specified	not specified	4.0 ± 0.5
charging plate size	larger than DUT	7 times larger (area) than DUT	**not specified**	**not specified**

The decision to define CDM ESD tester parameters implicitly by waveform requirements has been consciously made by the standards committees to ensure manufacturability of the CDM testers and at the same time ensure integrity of the waveforms. But this implicit specification causes additional variations in the discharge current waveforms since the tester manufacturers have been given a high degree of freedom to design and specify the setup parameters for the CDM testers. They can implement different combinations of ground plane size, field charging plate size and pogo pin length and inductive and capacitive parasitics to produce waveforms that comply with a certain standard. However, the stress imposed to a real product under test can vary significantly for the different tester setups. Unfortunately, critical setup parameters that would have allowed the development of repeatable simulations have not been clearly defined in the standard documents.

Charge Plate and Ground Plane Size

The recent work of Jahanzeb [11] [Figure C7 and Figure C10], Atwood [16], [Figure C8], and Goëau [17] shows that the size of the ground plane and the field charging plate can have a significant influence on the CDM discharge peak currents for ultra large packages. For smaller packages, when the charging plate and ground plane are much larger than the IC device, the CDM peak current increases linearly with increasing capacitance of the device under test. When the capacitance between the device under test to the field charging plate exceeds the capacitance formed between ground plane and field charging plate, the CDM peak current saturates as illustrated in Figure C7 [11] and Figure C8 [16].

For very large IC devices, where the package size approximates the size of the field charging plate and ground plane, the CDM peak current is not constant, but can vary depending on the pin position due to variations in the electrical field, as depicted in Figure C10 [11]. The highest peak currents are near the center of the large package due to uniform electric field lines, while the currents are lower along the edges of the die as the electric field lines are affected by fringe effects caused by the large size of the package.

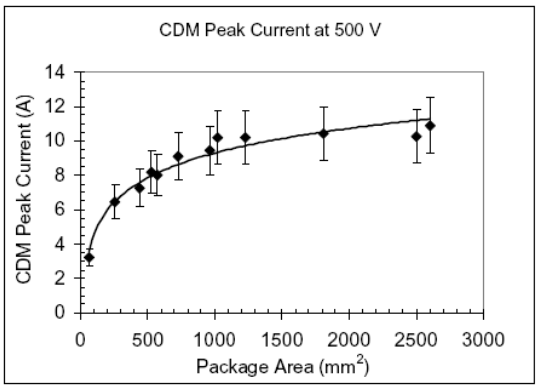

Figure C7 (Jahanzeb et al.[11]): Plot of peak CDM current (ESDA) for devices with varying package area. For package areas up to 1000 mm^2 there is an approximately linear relationship, while the peak currents for larger packages show a saturating trend.

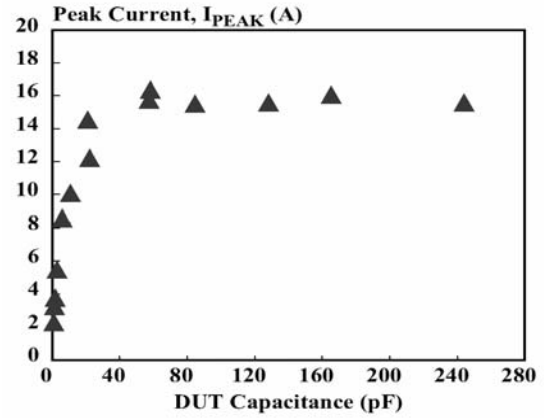

Figure C8 (Atwood et al.[16]): Peak Current versus DUT capacitance to field charging plane from a tester set up for JEDEC tests.

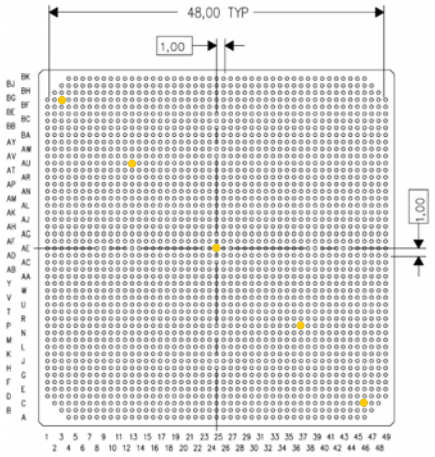

Figure C9 (Jahanzeb et al.[11]): Outline of a BGA package used for studying the CDM current profile for different pin positions. All dimensions shown are in millimeters. Package size is 50 mm x 50 mm.

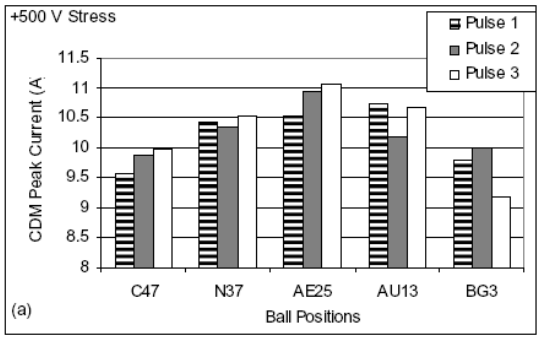

Figure C10 (Jahanzeb et al.[11]): CDM peak current variations at +500V (JEDEC) at different positions along the diagonal of the 50 mm x 50 mm package from Figure C9. The area of the applied charging plate is 126.6 cm^2 which results in a ratio of charging plate to package size of 5:1 (ESDA requires at least 7:1). The area of the ground plane is less than 50 cm^2.

C.3.2 Allowed Variability in Tester Setup Parameters

Today's non-socketed CDM ESD test standards permit a diverse range of setup conditions required to operate the CDM ESD test equipment. As a result, the ESD test results can vary among different tester setup conditions, even when IC devices are tested on the same test equipment using the same CDM standard.

A. Oscilloscope Bandwidth

The current oscilloscope requirements specified in the CDM standards are now out of date. New research shows that discharge current waveform using a 1 GHz oscilloscope are unable to capture the important CDM discharge waveform properties [10].

When the original CDM specifications were written a 1 GHz oscilloscope was the highest bandwidth oscilloscope that could reasonably be required in a testing laboratory due to

economic issues. This speed oscilloscope was capable of demonstrating the day-to-day functionality of the CDM tester at least for the lower frequency properties of the fast transient current pulse. As the price of high bandwidth oscilloscopes dropped and availability became more common, new measurements of the higher frequency uncovered disparate properties of the existing CDM simulators (Figure C11 and Figure C12). Consequently, signals can appear very similar when measured with the 1GHz oscilloscope, while they can look very different when measured with a 6GHz oscilloscope.

Today's standards allow the use of limited bandwidth oscilloscopes (JEDEC, AEC: 1GHz, ESDA: 1GHz or 3.5GHz, JEITA: ≥2GHz) to capture the CDM waveform. These relatively low bandwidth oscilloscopes are unable to capture the true CDM discharge waveform [10], as the lower bandwidth masks higher frequency signals in the CDM discharge waveform (compare Figure C11 and Figure C12). Consequently, signals can appear very similar when measured with the 1GHz oscilloscope, while they can look very different when measured with a 6GHz oscilloscope. These hidden differences can lead to different product test results between different testers or tester setups, even if the waveform captured from these testers with a lower bandwidth oscilloscope appear to be very similar. In fact, in order to meet the requirements of the current JEDEC JESD22-C101D standard, additional ferrite beads or alternate measures are typically employed in the discharge path for tuning the peak current, pulse width and rise time of the pulse. These parasitics, which are intentionally added to meet the specification requirements, cause significant distortion in the waveform, as can be observed in Figure C12. A "clean" waveform signal is measured with the limited 1GHz bandwidth oscilloscope as shown in Figure C11.

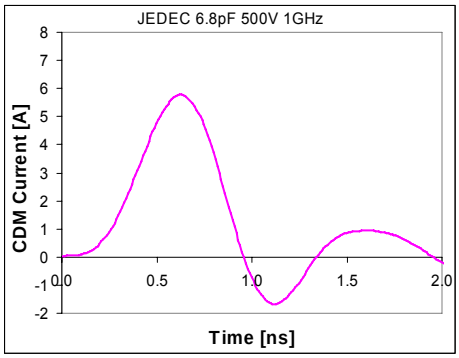

Figure C11: CDM discharge waveform, captured with a 1GHz (5GS/sec) Tektronix oscilloscope: JEDEC standard, Oryx Orion CDM tester, 6.8pF verification module, 500V.

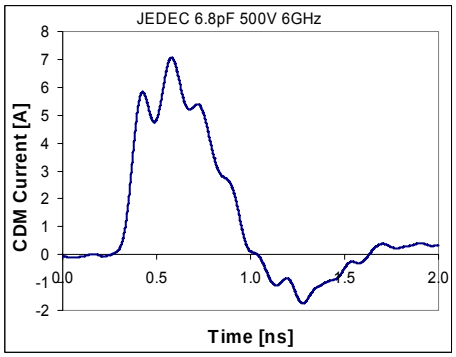

Figure C12: CDM discharge waveform, captured with a 6GHz (10GS/sec) Tektronix oscilloscope: JEDEC standard, Oryx Orion CDM tester, 6.8pF verification module, 500V.

B. Peak Current Range

The standards allow for a wide range of variation in the waveform shape. For example, all standards allow for a significant variation of the measured peak current during a discharge on the verification module from the nominal peak current: ±10% (JEITA), ±15% (JEDEC), and ±20% (ESDA, AEC).

When the standards were first developed the properties of the simulators were not well understood so large variations in the peak currents were acceptable. Today, many of the critical setup parameters are better known, but specific equipment improvements have not yet been implemented. This is a serious weakness in the existing CDM standards. As the IC device sensitivity levels decreases, the variations in I_{peak} will make accurate measurements extremely difficult.
As a consequence of the wide variations in I_{peak}, testers can be set up at the lower end or higher end of the allowed current window and the same tester can stress a device with a significantly higher peak current, depending on the setup. An example for the range of allowed peak currents in the JEDEC standard is depicted in Figure C13.

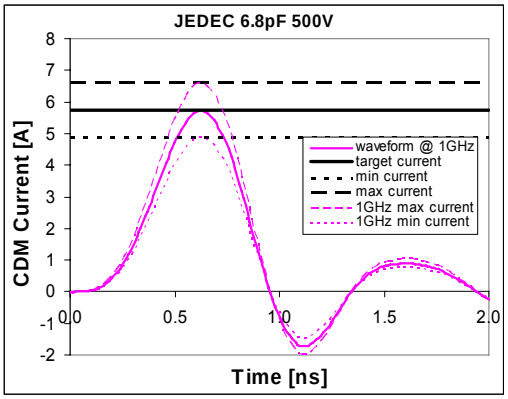

Figure C13: CDM discharge waveform for the JEDEC 6.8pF verification module at 500V with target, maximum and minimum allowed peak current for measurement with a 1GHz oscilloscope.

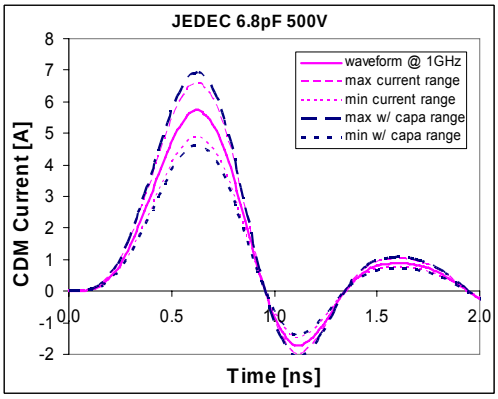

Figure C14: CDM discharge waveforms as in Figure C13. The blue waveforms show minimum and maximum currents when verification module capacitance variations in allowed range are considered.

C. Verification Module Variance

The wide acceptable difference in the peak currents is compounded by the permissible variations in the verification modules. The acceptable capacitance variations in the modules allow for a ± 5% deviation from the nominal capacitance value of the verification modules (see Table C-VIII). The Standards specifications are also very inconsistent as one specifies a metal coin while the other defines a metal film on a FR-4 dielectric.

When the effects of the peak current and verification variation are combined, the allowed peak current range can vary as much as ±20% for JEDEC, ±25% for ESDA and AEC.
As an example, Figure C14 shows the variations in the peak current for different tester setups. The peak current could be as low as 4.6 A for one tester and as high as 6.9 A for the same tester if an IC device with a capacitance to the CDM tester field charging plate of about 4pF was tested at 500V using the CDM JEDEC standard. This worst case minimum and maximum peak current level meet the existing ± 20% I_{peak} range. As a result, the pass or fail voltages would be extremely difficult to define, the IC device could be failing at 400V or passing at 600V. The acceptable variations in I_{peak} can result in inconsistent failure levels for the same pin tested on different CDM testers that are both in specification for the same CDM test standard.

Table C-VIII: Verification module parameters defined in the different standards.

Organization	JEDEC	ESDA	AEC	JEITA
capacitance	6.8pF±5% 55pF±5%	4pF±5% 30pF±5%	4pF±0.2pF 30pF±1.5pF	value not specified, only size

C.3.3 Nature of CDM Test: Non-Repeatability Issues

The non-socketed CDM tests as specified in the various CDM standards (Table C-I) require or allow either a "non-contact mode" or "air" discharge mode of operation, where the discharge occurs across a small air gap after the air dielectric breaks down between the test pin and the approaching discharge pin. This discharging method represents the actual discharge conditions as they occur in reality more closely than a "contact mode" discharge where the discharge is initiated within a mercury relay.

The major drawback of the non-contact mode discharge method is that the properties of the discharge arc are influenced by both test equipment and environmental factors. The material, surface area, and geometries of the CDM pogo pin and device pins, the approach velocity of the pogo pin, and climatic conditions such as temperature and humidity all combine to influence the discharge current waveform properties. In addition to that, the formation of the spark is a statistical process; the resistance can vary significantly from discharge-to-discharge.

Furthermore, when testing IC devices with very small pin-to-pin spacing at higher voltages, discharging to a specific pin can be problematic as making a contact with the small device pins is difficult and arcing to neighboring pins is likely. Reducing the size of the pogo pin's dimensions does not help as the electric fields around the electrode tip's head increases dramatically as the head is made smaller. The higher electric fields cause a premature dielectric breakdown at variable distances between the pogo pin and the pin under test. This variation can introduce an unpredictable arc resistance which can cause additional oscillations in the peak current values.

The available commercial CDM stress simulators are design to reproduce the CDM event as realistically as possible. The large deviations in the discharge currents resulting from non-contact mode discharges are currently accepted in the industry.

There can be significant variations in the CDM peak discharge current when a product is stressed several times on the exact same pin. In Figure C15 and Figure C16 Jahanzeb [11] and Brodbeck [12] show significant peak current variations ranging by ± 20% in the first paper and + 25% and - 60% for the second paper. This data clearly illustrates the extreme statistical variation in the arc discharge within the stress of a single pin.

If the ground pogo pin discharges on different positions on the IC device's lead finger [Figure C17] then the rise time, peak current and pulse frequencies are also affected [12]. For the same applied voltages (500V), the JEDEC and ESDA methods release different maximum peak currents [12]. Figure C18 shows that the peak current values for all 256 pins of a LF-BGA-256 package. The data illustrates that the ESDA standard produces 20

– 30% higher maximum peak currents compared to the JEDEC standard test method and that the maximum peak current varies significantly from pin to pin.

The variation in arc resistance is illustrated in Figure C19 where the peak currents of the JEDEC 6.8 pF calibration module are compared to A1 ball on a BGA package.

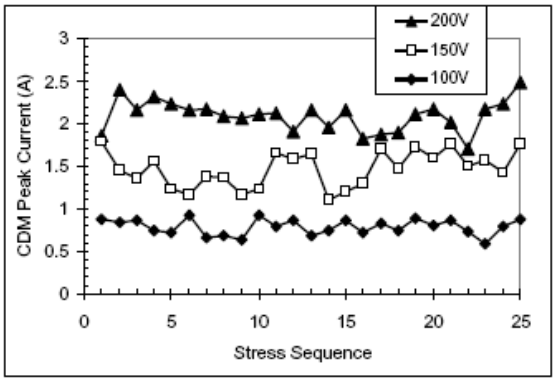

Figure C15 (Jahanzeb et al.[11]): Peak CDM discharge current for a sequence of 25 pulses on the same pin. The variation of the discharge current is depicted for three different CDM voltages. The device package size is 10 mm x 10 mm.

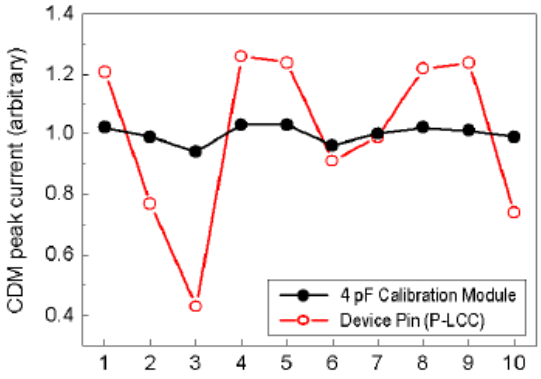

Figure C16 (Brodbeck et al.[12]): Normalized CDM discharge peak currents for a component (P-LCC) and a verification module (4-pF-ESDA) for ten consecutive discharges (RCDM, 1.5 kV, 60% RH).

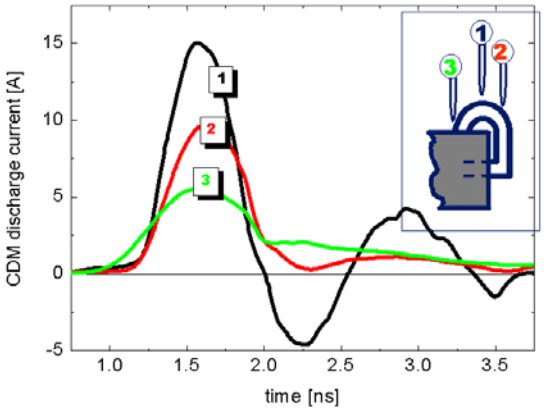

Figure C17 (Brodbeck et al.[12]): CDM discharge current waveforms for three different positions between the discharge pin of the test system and the pin of the device (RCDM, ESDA mode, 60% RH).

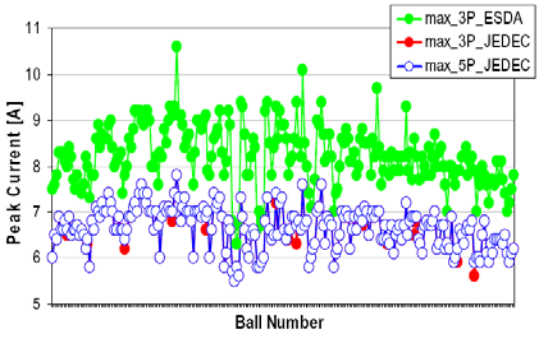

Figure C18 (Brodbeck et al.[12]): CDM discharge current peak current for different balls on one package for ESDA and JEDEC. The maximum peak current of three (3P) or five (5P) CDM discharges is depicted.

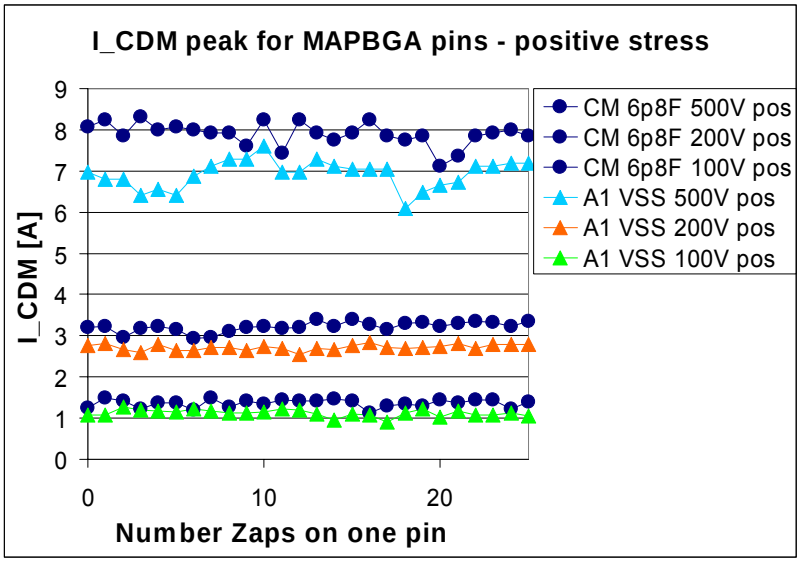

Figure C19: CDM discharge peak current for several discharges (JEDEC) on the same calibration module (6.8pF) and the same BGA package pin (A1-VSS), respectively. Peak currents are shown for 26 consecutive zaps at three different voltage levels (100V, 200V, and 500V). A large variation of the peak currents can be observed.

C.3.4. Correlation Data for Different CDM Testers with the same Standard

CDM ESD correlation study was performed at ESD labs at Freescale using 130 nm CMOS IC devices. All devices were tested according to the JESD22-C101D standard. The purpose of the correlation study was to compare CDM failure levels for the same IC devices tested on multiple CDM testers in different labs. CDM discharge current waveforms using the verification module measured before and during the evaluation tests met the JEDEC standard specification. The test results showed the lowest failing voltage was at 650V for units tested on Tester1 in Lab 3, while units tested in Lab 1 and Lab 2 passed voltages as high as 750V. The test results differences [Table C-IX] were greater than 150V among the different fully calibrated test equipment. Measuring the peak currents resulting in a failure on calibrated systems would have provided deeper insight and would likely have explained the discrepancy in the test results.

Table C-IX: Freescale's JEDEC Multiple ESD Lab Correlation Test Results

	250V	**500V**	**550V**	**600V**	**650V**	**700V**	**750V**	**1000V**
ESD Lab1	pass	pass	n/a	n/a	n/a	n/a	pass	fail
ESD Lab2	pass	pass	n/a	n/a	n/a	n/a	pass	fail
ESD Lab3/Tester1	pass	pass	pass	pass	fail	fail	fail	fail
ESD Lab3/Tester2	n/a	n/a	pass	pass	pass	pass	n/a	n/a
ESD Lab4	pass	pass	n/a	n/a	n/a	n/a	fail	fail

C.3.5 Conclusions for Current Test Methods and Standards

The existing CDM standards (JEDEC, ESDA, AEC or JEITA) permit too much variation in critical discharge current waveform parameters, like peak current. Some of the error is intrinsic to the air discharge, but the primary reason for this error is due to inadequate

tester specifications. None of the existing standards provide adequate specifications for pogo pin length, charging plate size, tester head model, and ground plane size [10][11][16]. The approach speed of the pogo pin is not well defined and humidity controls are missing. As a result, the CDM test results of the same product (and package) can differ significantly depending on what CDM tester type (e.g. manufacturer, model, and year) and setup parameters were used for the test. Achieving repeatable and reproducible CDM test results will become even more challenging when the CDM sensitivity levels decrease for advanced 65 nm and 45 nm technologies.

The existing CDM (non-socketed) standards for many years have accepted the non-contact mode or air discharge mode of operation. This type of test method attempts to model the "real" CDM discharge event even though this type of discharge event produces peak currents that are variable and erratic. The air discharge ESD event is intrinsically more inconsistent because of fundamental environmental issues which influence the discharge current waveforms.

When these basic properties are combined with advanced design of high pin IC devices with extremely tight ball-to-ball pitches, the success rate for achieving highly repeatable test results is low. When the voltage steps are 100V or less, determining an actual CDM pass or fail voltage is very difficult. The variability that exists on one CDM simulator for a single IC device is increased when simulator-to-simulator variation is included for the same type and design of simulator. When different designs of manufactured CDM test equipment are compared, the variability factor increases to an even higher degree of unpredictability.

The goal of reproducing "real world" CDM discharges comes with a very high price; the primary casualty is achieving very tight repeatability and reproducibility of the ESD discharge event.

C.4 Issues caused by Voltage Classification Levels

All existing ESD standards include classification levels that are based on voltage requirements. For example, if a device withstands an HBM stress of 1000V the ESDA HBM standard classifies this device at Class 1C level. For HBM, the stress a device experiences at this 1kV level is about the same, independent on the package size and type the IC is using, and independent on what standard is applied or what tester manufacturer is used. This is consistent with the definition of any standards classification level, which is to rank the relative ESD sensitivity levels to a fixed stress condition.

For CDM, this is not the case. The CDM standards include sensitivity levels as well. For example if a device withstands CDM stress of 500V or more in the ESDA standard, the ESDA CDM standard classifies this device at a C4 level. However, if the same device is tested in a larger or thinner package with a larger package capacitance, the same device will likely not be able to pass 500V CDM stress. Consequently, devices in larger, thinner packages have to withstand a much higher stress in terms of current to qualify at the same voltage classification level. If tested to a certain CDM voltage level, larger and thinner packages fail at a much lower voltage than the smaller and thicker packages.

This fact makes it very difficult to impossible to design on-chip ESD protection for any IC as ESD protection has to be designed according to the expected current during an ESD event. For HBM, this current is about the same for a certain voltage level or classification level, but for CDM, that peak current can vary widely from DUT-to-DUT, depending on die and package size.

C.5 Conclusions

This appendix briefly compared the different CDM ESD test methods and standards including JESD22-C101D, ANSI/ESD STM3.1-1999, AEC-Q-100-011REV-B and EIAJ ED-4701/300-2 Test Method 305. The analysis has clearly shown that the specific set-up parameters for each of these CDM standards vary significantly. In addition, the individual verification modules are built with different materials and capacitances. As a result, a different stress is applied to the device under test for each standard model. Consequently, the CDM pass or fail voltages vary significantly for the different standards and cannot be easily compared among these standards. When CDM ESD test results are discussed for a certain IC device, the standard for which the units were tested should always be considered. Applying a simple scaling ratio among the different standards would most likely produce very inconsistent and incompatible results.

Performing CDM ESD test is much more complex than the HBM component level test. The air discharge ESD event intrinsically produces peak currents that have a significant statistical variation. Many external environmental factors, like humidity, temperature, size and shape of the IC pin or ball and the diameter of the ground pogo pin, strongly influence the air discharge current waveform parameters. Although the existing CDM standards define some of the critical setup parameters, variations in peak currents produced by all of the CDM test simulators show that there are still critical parameters that are not adequately defined. This reproducibility and repeatability problem is highlighted by the acceptable peak current variations in each standard: ± 10% (JEITA), ± 15% (JEDEC), and ± 20% (ESDA, AEC). The lack of control of these environmental variables contributes to a wide range of peak current variations. Future revisions of the standard documents should include a definition of these parameters to reduce the variability in the peak discharge current. In a new revision of the existing standard documents, these parameters should be more closely defined to reduce variations in the peak current to a minimum level. Waveforms should be measured and system verification should be done with an oscilloscope with a bandwidth significantly above 1GHz, e.g. 6GHz. Waveforms measured on verification modules with a verified correct capacitance value should be provided with each CDM ESD product test. Today, CDM discharge currents at lower CDM stress voltages (e.g. 100V or 200V) are somewhat more consistent.

All CDM industry standards include classification levels that are based on voltage requirements. For the HBM model, which applies stress voltages to a fixed external capacitor, a certain voltage level results in a fairly well defined current stress level for a device under test. However, for CDM, the stress voltage is applied to a package capacitance. This capacitance is a property of the IC device and is variable, depending on

package size and thickness. Consequently, devices in larger, thinner packages have to withstand a much higher stress in terms of current to qualify at the same voltage level. If tested to a certain CDM voltage level, larger and thinner packages fail at a much lower voltage than the smaller and thicker packages. This fact makes it very difficult to impossible to design on-chip ESD protection for any IC as ESD protection has to be designed according to the expected current during an ESD event.

C.6 Outlook

Devices with a potential weakness with respect to CDM ESD need to be identified as early as possible, while the fundamental issues with reproducibility and correlation described previously in this appendix should be avoided. Therefore methods are required that reproduce the electrical and physical failure signatures of a CDM-like ESD event at well defined stress levels. This test should preferably be performed as soon as silicon is available, i.e. the test should be enabled on wafer level as well as on the packaged IC device.

One method that can meet these requirements is called Capacitive Coupled Transmission Line Pulse (cc-TLP) which was introduced by Gieser et al. [4] and Wolf et al. [5] (see Figure C20 and Figure C21). The cc-TLP test method was successfully applied to generate CDM type failure signatures for packaged IC devices and also for devices on wafer level. A good correlation of peak stress currents leading to failure was observed between cc-TLP and CDM for CMOS technologies down to 90 nm (compare Figure C22).

For cc-TLP testing, a very reproducible, rapidly rising square pulse, which is generated in a vf-TLP, is injected into a single stress pin, after an electrical contact is established to this pin. The exponentially decaying charging current (RC) distributes over the full device under test similar to a rapid charging during FCDM testing and generates voltage drops internal to the device very similar to a FCDM stress. While the stress test of the final package is necessary for qualification, a first determination of the robustness of a product at wafer level is very helpful in short design cycles. This method may be applied to packaged IC devices to produce results with a high repeatability and consistency and to compare the overall robustness of different IC devices to CDM-like ESD events. With this in mind, cc-TLP's suitability as a replacement for traditional CDM warrants serious consideration.

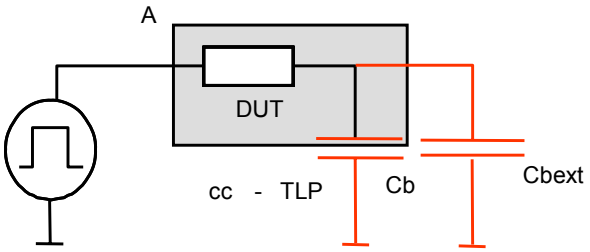

Figure C20: Principle of cc-TLP test. cc-TLP is a one pin stress. The stress current of the device under test depends on the amplitude and rise time of the vf-TLP pulse used for this test and on the capacitances.

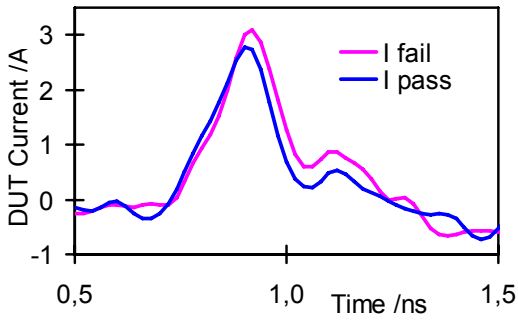

Figure C21: cc-TLP current waveforms for two pulses with increasing voltage levels. The device still passes after the lower pulse, but fails after it was stressed with a slightly higher pulse.

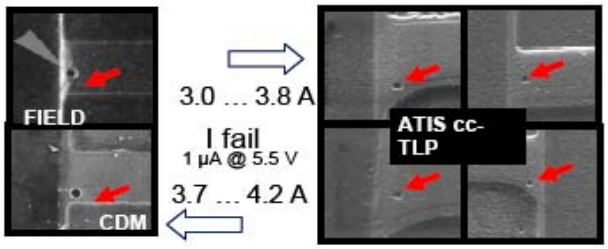

Figure C22: Comparison of physical failure signatures in field, and from CDM and cc-TLP test. cc-TLP reproduced the gate oxide failure signature of failures from the field and after CDM ESD test.

C.7 Acknowledgments

The authors would like to thank Horst Gieser and Henry Wolf of Fraunhofer Institute in Munich for providing the information about cc-TLP included in this appendix.

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Appendix D: CDM – Does it Correlate to Other ESD Stresses?

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Leo G. Henry, ESD/TLP Consulting, Teaching & Testing
Benjamin van Camp, Sarnoff Europe

This appendix addresses possible relationships between CDM [1] and other ESD-like phenomena. Therefore it explores the correlation between CDM and the other component level tests, HBM [2] and MM [3]. It has been shown that HBM and MM are generally very well correlated [4]. In the spirit of conciseness, we will therefore only refer to HBM when comparing to CDM. Further the correlation to other tests or phenomena, such as system level ESD [5], Charged Board events [6], and EOS are discussed. The analysis will start from a theoretical point of view and will be illustrated by examples and case studies. Finally the conclusion will summarize the consequences for the recommendations.

D.1 Theoretical Analysis

ESD failures arise due to two distinct mechanisms: high local power dissipation and breakdown due to high electrical fields. The first mechanism typically leads to damage due to melting / dislocation of material. The second mechanism typically leads to damage in dielectrics or as a trigger for the first mechanism. Obviously the nature of the damage will depend on the available energy and the location of the dissipation. A study of possible correlations between ESD-like phenomena therefore requires that the electrical parameters determining the conditions for the failure mode need to be compared.

Thermal failures depend on the energy content of the discharge, the power in the discharge and the duration of the discharge. The latter two are related via the so-called (non-linear) Wunsch-Bell relation [7]. Dielectric failures are due to high electrical fields, i.e. high voltage differences in the network. These arise from two reasons. First there is the large peak current. Second, the dv/dt of the discharge event induces high peak voltages on ESD protection circuits prior to turn on [8].

Relevant parameters describing the different phenomena, such as energy content, pulse width, rise time and peak currents differ significantly. Some of these parameters are defined mainly by the method, e.g. in the case of HBM while others depend significantly on the DUT, e.g. in the case of CDM. Table D-I summarizes the fixed parameters and calculated quantities for a 1 kV event for all phenomena. Where applicable the values are given for realistic range of DUT parameters. Clearly there are large differences between the models. The consequences will be discussed in the next sections.

There are significant differences in how the discharge currents are distributed within the DUT, due to the different nature of the test mechanisms. Many of the phenomena can be

described by a 2-pin experiment. The discharge current enters the DUT at a given pin and exits at another pin. In a normally designed ESD protection network, these tests evaluate robustness of predefined paths specifically designed with ESD current capability in mind. For CDM however, one of the pins is the capacitive coupling of the DUT to the outside world/tester. The energy of the pulse is stored in the chip / package capacitance itself, as the reference voltage of the chip is different than ground. A discharge to ground of any one pin causes a multitude of parallel paths of current within an IC. The CDM path of discharge is from the internal circuit out, and internal circuitry derives a voltage from the power and ground domain capacitance developing a voltage from the pin discharge. Due to different delay times this may generate voltage differences over devices.

Table D-I: Comparison of some typical network values and electrical quantities for a 1kV stress.

	C (pF)	R (Ω)	τ (ns)	Q (nC)	E (μJ)	P (kW)	Ip (A)
HBM	100	1500	150	100	50	0.330	0.67
CDM	1-100		1-2	1-100	0.5-50	0.25-25	1-25
System	150	330	50	0.15	75	1.5	3.0

D.1.1. HBM vs. CDM

It is well known that the time constant associated with CDM is much smaller than that of HBM. The difference is so large that the two types of stress may actually address two different regions in the Wunsch-Bell diagram. As is clear in Table D-I, the peak current for CDM can be much higher than for HBM. Thus even assuming all power is dissipated in a single location, it is clear there will not be a strong relation in general between CDM and HBM. Second, the high dv/dt of the CDM discharge event induces higher peak voltages on ESD protection circuits prior to turn on [8]. Therefore internal gate oxides of cross-domain logic can be exposed to high voltages for a slightly longer time in nanoseconds before full discharge, and thus more prone to damage.

It is generally observed that most of the samples that fail a CDM test show gate oxide failures, where as samples failing a HBM test show melt failures. Thus a correlation between HBM and CDM is not expected. The next section will show this by FA examples and a correlation calculation.

D.1.2. System Level ESD vs. CDM

The history and model of System level ESD (IEC) is described in Chapter 7 of Industry Council White Paper 1 [4] and the IEC 61000-4-2 Standard [5]. It is well-known that the unique feature of the System Level ESD waveform is that it is composed of two distinct portions, the first a very fast (~ 1 ns) high peak current portion and the second a medium speed (10-100 ns) medium current portion. The initial portion resembles the first peak of a CDM-like waveform where large potential difference tends to be generated. The second portion is similar to HBM or the first peak of MM stress that has more energy. It should be noted that this holds for a calibration waveform of the ESD gun into a defined short. Depending on the system board circuit and system pin of discharge, the energy seen by the board will be different in different parts of the board as the paths taken can vary, and the failure mode is not predictable.

It has been shown that system level pulses can produce failures that look like CDM damage as well as failures that look like HBM damage. This has been shown on products

[9] and on test structures [10], as shown in Figure D1. Although the physical mechanisms of the damage are the same as those that occur during product qualification, it is in general not possible to relate product and component level results. The failure mode of the IC in the system, as well as the failure voltage depends on the printed circuit board (PCB) design and way to assemble the system.

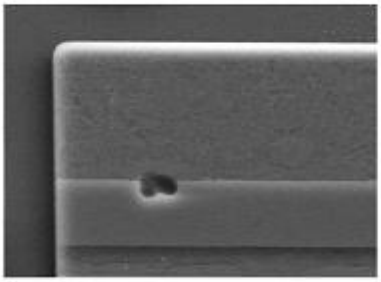
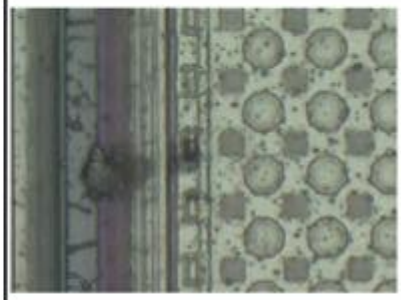
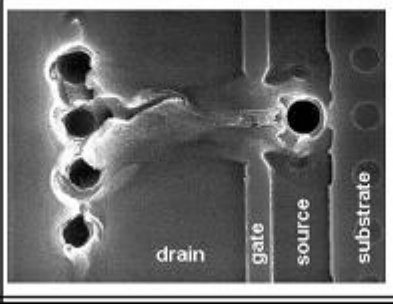
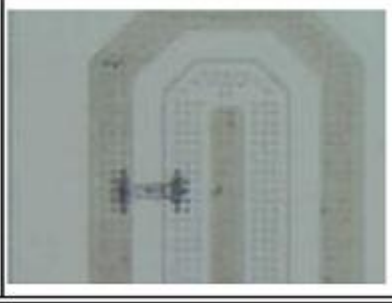
Failure mechanism	failure device level	failure system level
Breakdown of an isolation (left: gate oxide, right: LOCOS)		
Thermal melting of silicon		

Figure D1: Different failure modes from component level and system level stress [9]

This is why the Standard Setup for System Level Test, as it relates to stressing certain pins of ICs on a board, is being developed [11]. In addition, as described in White Paper 1, it is known that EMI generated by system level ESD test may cause latch-up like failures that cannot be caused by the device level ESD test since these are always done in un-powered mode of the IC. Typically these do not lead to physical damage, but if they do they will be of the thermal category.

D.1.3. CDM vs. EOS

The term EOS stands for "electrical overstress". For electronic components, overstress is divided into two general energy spectra: ESD, which applies to overstress signals less than 1 µs in duration, and EOS which covers overstresses beyond 1 µs in duration [7]. ESD manufacturing controls (in machines, equipment and of personnel) will prevent EOS events. However, when electronics come in contact with materials that are unprotected or otherwise have a voltage on them, discharge into the circuitry can occur which can cause an EOS event. Examples of EOS events include unpowered devices inserted into "hot" test sockets with voltages applied to them, or improper power supply sequencing. The latchup test [12] applied to integrated circuits qualifies as an EOS event as it is performed at voltage above that of normal operation for durations up to several milliseconds. However, shorter overstress events of higher voltage, or longer overstress events, can cause EOS damage.

The total energy of CDM events is much below that of the transition between an ESD and EOS event. The failure modes seen in CDM demonstrate this, as the damage is normally much less extensive in area and material impact than that of an EOS event. The clear distinction between the failures ascribed to Electrical Overstress (EOS) and the failures ascribed to Electro-Static Discharge (ESD) have been demonstrated [13] [14]. The mechanisms associated with the ESD current flows through the chip have been demonstrated [15] [16]. The mechanisms associated with the EOS failure have also been demonstrated [17], where EOS failures occur mostly in the bond wires (burnt, fused), on the die surface (glass and top metal) in the form of deformed glass on burnt/fused metallization. This is characterized mainly by discoloration at the site of the failure. This is in direct contrast to the lack of discoloration characteristic of ESD failures in general and CDM failures in particular. For EOS, low magnification (up to 1000X) is enough to see the failures while for ESD, very high magnification is required. The ESD failed device must be deprocessed down to the silicon level. Since the ESD and EOS simulations require different pulse width and rise times, there is no correlation expected.

D.1.4. CDM vs. Charged Board Event

CDM failures result from discharge of stored charge in the device capacitance. The device capacitance, which is charged as a result of the CDM event depends on chip size and package size, and is typically a few tens of pF at most. On the other hand, in CBE, the relevant capacitance depends not only on the device and package but also on common system board capacitance and other IC capacitances connected to it [6]. So, CBE total capacitance around the IC is much higher than the single DUT CDM case. Because this large amount of charge discharges through some IC in a CBE discharge, discharge current may be several tens of times more than the device level CDM and are more likely to produce thermal failures than CDM [18]. More details are given in Appendix E.

D.2 Example and case studies

In previous sections of this appendix the differences between CDM and other ESD models have been described. These differences include the energy / duration of the pulse, the source of the energy and the generated failure modes. Thus we need to compare FA from CDM and otherwise stressed samples. This section will describe classic failure types observed from CDM tests and compare / contrast this to those of the other failure types.

D.2.1. CDM

Figure D2 shows two photos of typical CDM damage. Figure D2a is a -500V CDM failure illustrating a classic CDM failure type involving the gate / source of two NMOS transistors in one domain whose gate is driven by logic from another domain. Figure D2b is a result from a –300V CDM failure on an input buffer. It should be noted that in both cases the transistor is small and while the damage is clearly visible, it only takes a relatively small amount of current to cause this damage.

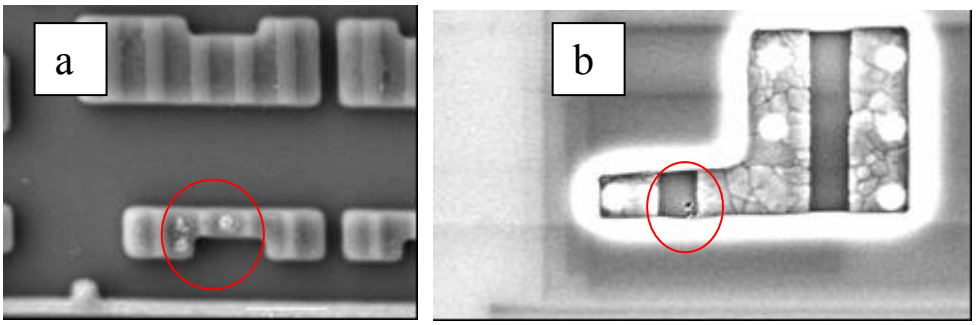


Figure D2: CDM failures of two NMOS transistor gates driven by cross-domain logic (a) and an input transistor (b).

D.2.2. HBM

Figure D3 shows two HBM failures. Figure D3a is a 2 kV HBM failure illustrating a classic HBM failure type involving the drain / backgate junction of a larger MOS I/O transistor. The current path of this zap was a positive zap between the damaged pin and a nearby ground pin. Figure D3b is the failure of a core transistor for a stress between Vdd and Vss.

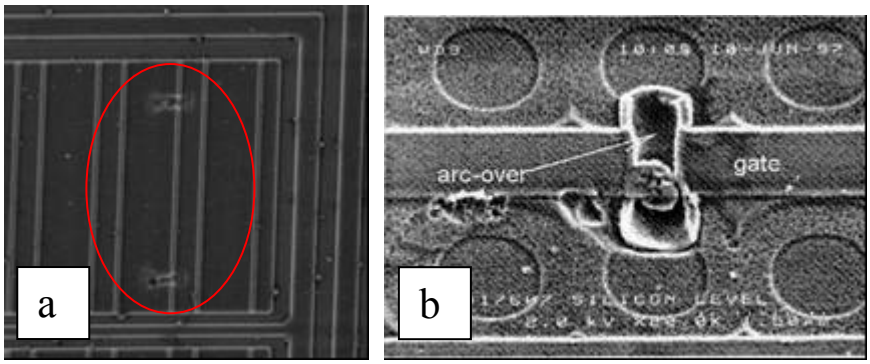


Figure D3: 2 kV HBM failures showing contact spiking / silicon damage.

Without a doubt, CDM failures look very different from the HBM failures and they occur at different locations on the chip. Electrical and ESD Simulation testing of these failures can show both leakage and functional changes, and are not sufficient to determine the root cause of a field return. FA must be performed on product returns to find similarity with qualification fails.

It is clear that a correlation between HBM and CDM is not expected. A scatter plot of data of many products from different manufacturers, presented in Figure D4, makes clear that indeed a correlation is not observed. The correlation coefficient is just 0.26, which is equal to the correlation observed on a totally unrelated dataset in [14].

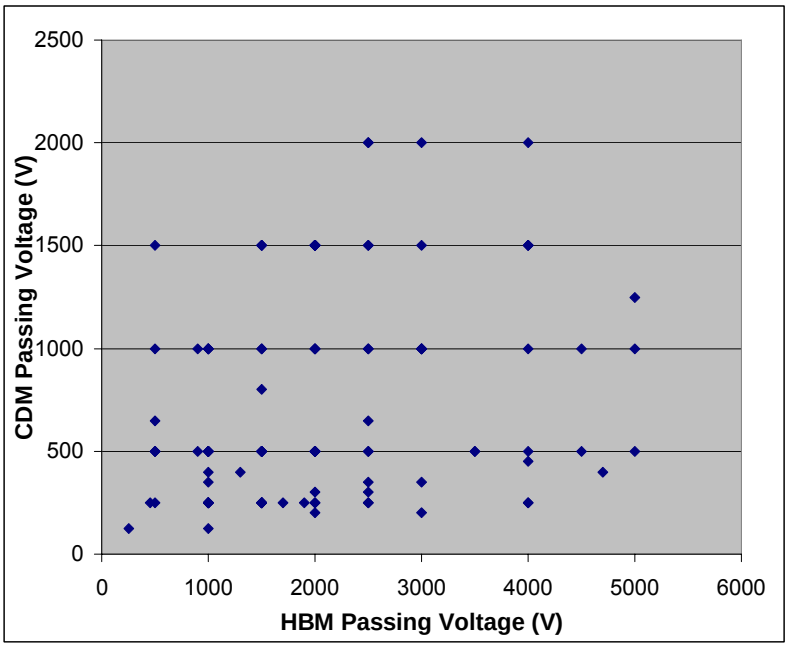


Figure D4: CDM vs. HBM levels for >100 different products.

D.2.3. System Level ESD

Some case studies that show little correlation between CDM failures and System Level (IEC) failures will now be discussed.

Case Study 1:

This case involved an IEC discharge directly applied to a device, where a CDM-like potential difference and high current resulted in failure at discharge to the enclosure. As the ESD gun discharged into the system enclosure, spark discharge was detected at a small gap between the enclosure and system PCB. This gap was close to a ground trace of the PCB where the damaged device's ground pin was connected. A power supply clamp between a power supply and ground was damaged as is shown in Figure D5a. The damage was caused by the uncontrolled discharge through the clamp, started by the spark. It was observed that the damage voltage was dependent on system enclosures, where the gap between the enclosure and PCB was varied.

Case Study 2:

This case resulted from direct discharge to a system board connector terminal, where no correlation to device CDM failure was observed. In this case, the connector contact was badly damaged as a result of high current applied to the terminal. An examination of the PCB revealed a printed circuit parasitic pattern from the connector to the device. The initial high frequency / high current portion was blocked off because this pattern worked as an inductance. When the applied waveform was measured at the IC, no initial pulse was detected. Only the second peak reached the IC. The resulting damage is shown in Figure D5b.

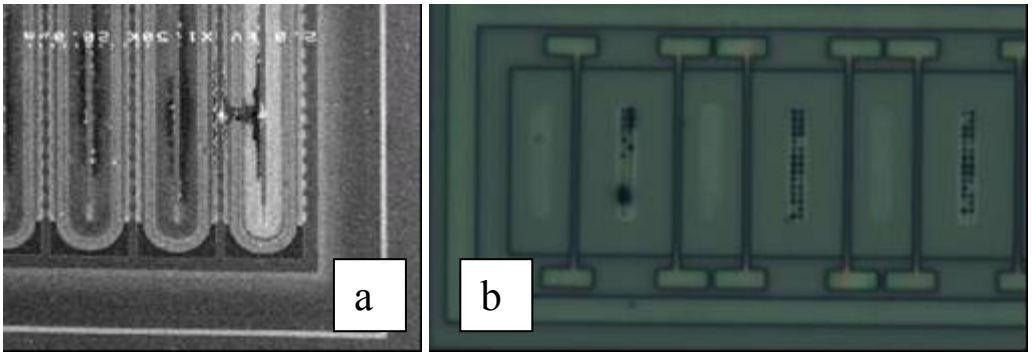


Figure D5: Damage in a power driver LDMOS (a) and damaged drain contacts of output buffer NMOST (b) due to system level ESD.

These case studies illustrate that non-correlation between CDM and System Level (IEC) was observed. Additionally, these studies illustrate that component level ESD protection alone is not sufficient to achieve high system level protection.

D.2.4. EOS

Two examples of EOS damage are shown in Figure D6. Figure D6a shows the result from a 2-pin test, with stress to the input pin with respect to ground. The stress was an over-voltage of 1.5*Vcc value, using a parametric analyzer. Figure D6b shows the damage due to a 1.5*Vdd stress on a power supply pin with respect to ground. This was performed while the device was other wise normally powered. The failure occurred in the core of the IC failure. The characteristic discoloration is easily observed.

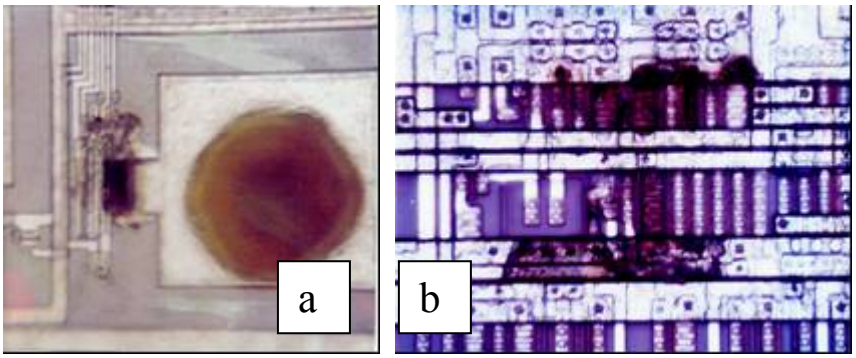


Figure D6: EOS failures, at input pin (a) and in core (b)

D.2.5. CBE

This case study involved melting of an ESD protection diode, shown in Figure D7, at the IC terminal of a device on a system board. A TLP tester was used to apply the stimulus to simulate the CBE. The failure charge of the diode was measured as 3.6A/100ns, corresponding to 360nC. Given the device capacitance of this IC was 12 pF, a 30 kV CDM event would be required to produce the same charge. This is much higher than levels achievable from a single component CDM test (1ns time constant discharge).

The PCB capacitance containing the IC was measured to be 20 times of the device capacitance, or, 240pF. The discharge time constant of this higher capacitance was 2.5 times that of the CDM time constant. If the PCB is charged at 500V, the total energy will

be the same level as above. This illustrates clearly that CBE is not correlated to CDM. Section E.5 gives more details on comparable case studies.

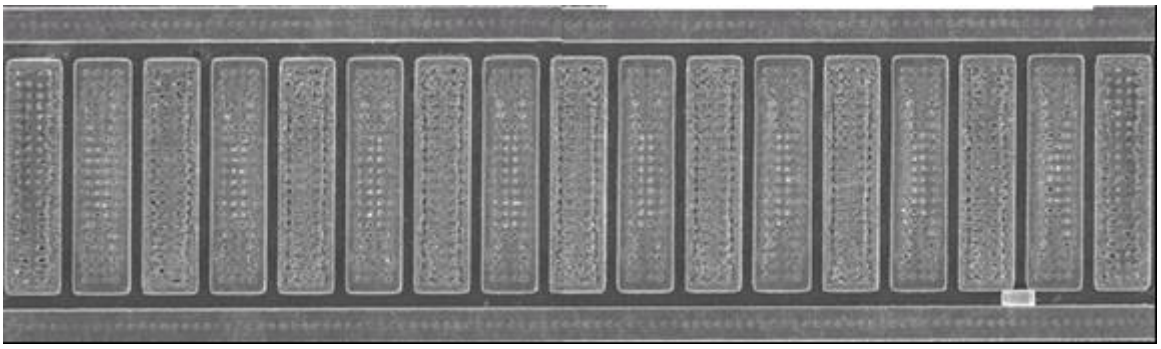


Figure D7: All contacts of the ESD protection diode were damaged.

D.3 Conclusions

This appendix shows that there is no correlation of CDM to any other stress types expected. Therefore CDM cannot be replaced by, nor replaces, any of the other stress types. An increased CDM level will not lead to higher performance for other stress types.

References

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Appendix E: Charged Board Events and Relationship to CDM

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E.1 Charged Board Event Problem Statement

Printed circuit board (PCB) ESD failures have received significant attention from the 1980s to today. The PCB ESD focus until recently has been largely on ESD protection at the system level which has been discussed in Appendix D as well as in the Industry Council on ESD Target Levels White Paper I.

There are four distinct mechanisms for discharge transients associated with a PCB [1]. In the first mechanism, if a charged person touches a PCB that is already grounded, the discharge transient represents HBM and the resulting damage will be HBM in nature. In the second mechanism, if a charged cable (which gets charged by triboelectric friction such as dragging) comes into contact with a grounded PCB, a cable discharge may result in a PCB component experiencing damage. In a third mechanism, if an ungrounded charged machine comes into contact with a grounded PCB, a component experiencing damage results from a machine model-like discharge. S20.20 does protect against cable discharge in ESD-controlled manufacturing environments, but for systems built for the non-ESD controlled environment of home or office, such systems should be ESD protected to withstand cable discharge.

Since the late 1980s, theory and evidence has indicated a fourth ESD threat mechanism due to charging / sudden discharging of system boards.

Pierce [2] initially described a relationship for ESD failure voltage by comparing the capacitance characteristics of a component versus a board and the failure voltage of a component, relating the ESD failure energy of a component to the system delivering the energy to the IC. For the same energy a much lower failure voltage was found to result. Boxleitner [3] in 1991 further described circuit board layout characteristics and variations in discharge paths to result in a wide variation in component failure voltage on a system board, down to $1/100^{th}$ of the failure voltage of the individual component. Lin [4] described AT&T work attempting to model a FICBM (Field-Induced Charged Board Model) discharge on a 6" by 12" circuit board, with hardware closely approximating common non-socketed CDM testers. A FICBM waveform specification for such a circuit board was developed including peak current, rise time and pulse width.

No standard model exists today describing the application and test conditions for a charged board event. The majority of the literature refers to the charged board event as Charged Board Model (CBM). However, the following discussion will retain the CBE nomenclature.

E.2 Charged Board Event (CBE) Overview

Conceptually, a CBE is similar to the Charged Device Model (CDM) event for a packaged component. During a CDM event, the charge stored by a packaged IC discharges just (nanoseconds to picoseconds) before contact is made with a conductive object at or near ground potential. During a CBE, the charge stored by an entire PCB discharges just (picoseconds to nanoseconds) before contact is made with a conductive object at or near ground potential. Thus, a CBE can be thought of as an extension of the Charged Device Model where the PCB is the "device" which stores the charge. However, since a PCB can store far more charge (due to higher board plane capacitance) than a single IC, the peak discharge current for a CBE is typically much higher compared to a CDM event. Consequently, the damage from a charged board discharge can be quite severe and can be easily mistaken for electrical overstress (EOS) damage.

There are three different methods to charge up a board, and similar means of discharge. In the first method, if an ungrounded PCB is held by a charged person and a metal component such as a bare metal heat sink is then exposed to a ground potential, any resulting component damage will be CBE in nature. In the second method, the off-board edge connector on the charged PCB usually makes contact with the card-frame connector into which the PCB is being pushed. The PCB rapidly discharges via whichever connector makes contact first, and the susceptible ICs in its path may fail. In a third method, board-mounted ICs can be damaged by the discharge current which flows when a charged PCB is grounded via wave soldering, an input connector, by an electrical tester, or contact with a metal object having a large capacitance. Here the PCB is in the electric field of a charged object or surface, the insulating materials on the PCB (such as plastic sockets, plastic covers or connectors) develop charge, the conductive portions of the PCB including the components develop voltage upon discharge by becoming grounded in the field from charged insulators on the board. Damage resulting from the discharge of this voltage to ground is also a charged board failure.

E.3 Relation of Charged Board Events to Component Level ESD Test Methods

Component-level electrostatic discharge (ESD) standard models in widespread use in the electronics industry include the Human Body Model (HBM) and the Charged Device Model (CDM). For integrated circuits (ICs), ESD testing to these models is conducted on an individual component basis, i.e., ICs are not mounted to a Printed Circuit Board (PCB) when stress tested for qualification. This component-level ESD testing is effective at simulating manual and automated real-world ESD events that occur on ICs prior to PCB mounting. However, component-level ESD testing is not a good predictor of how susceptible ICs are to ESD after they are mounted on a PCB. In fact, an IC mounted to a PCB may be much more or much less susceptible to ESD than when this same IC is handled individually. Supporting information can be found in Appendix D, Sections D.1.4 and D.2.5.

E.4 Charged Board and Related Failure Case Studies

Recent work details case studies of actual charged board events and lowered failure levels relating parasitics of a system compared to that of a component.

Olney [5] described the "Charged Strip Model" susceptibility of parts connected together as strips in an interconnected package leadframe. This susceptibility occurs when the individual pins are disconnected from the interconnected leadframe. Charge and subsequent discharge of disconnected pins (both from a tester pogo pin issue and on a cut down strip with a CDM tester) showed much lower failure strip CDM voltage levels compared to CDM levels of the individual components. The net capacitance of the collective leadframe connected packages is a function of the number of packages with the discharge path through the very low interconnected leadframe resistance / inductance.

This work led to a more detailed study [6] documenting unique ESD field failures of components assembled on boards. Two examples from this paper served to illustrate board charging issues during manufacturing resulting in severe ESD damage.

E.5 Example Charged Board Event Testing Methods

In [5] [6] a commercially available non-socketed CDM test system was used to test the strip, the specially designed CBE test board and a customer return board. This CBE methodology is acceptable as long as the board or board section fits inside the area of the field charging plate, which is generally less than 4 inches square. Figure E1a shows a photo of a board tested using the setup in [6].

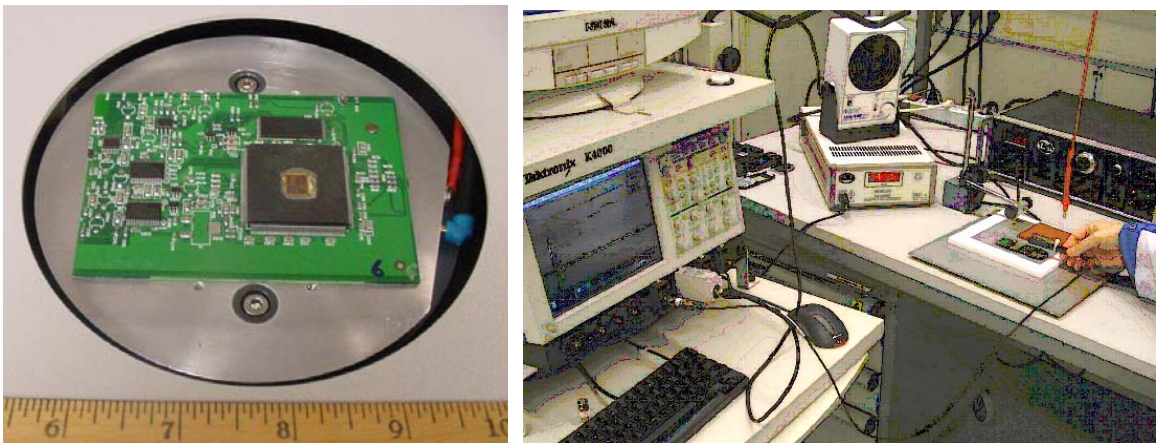

Figure E1a (left): Photo of customer PCB on commercial CDM tester. Figure E1b (right): Custom designed CBE evaluation system for PCBs.

A second setup used in the CBE evaluation of PCBs will now be described. The CBE ESD stress test principle can be used to validate ESD sensitive components on a system level. The method is adequate to evaluate ESD withstand of sub-assemblies and modules [7]. CBE withstand is valid also in the manufacturing environment and ESD risks can be

estimated by using electrostatic source circuit parameters such as capacitance, potential and charge.

The test setup for the CBE method is shown in Figure E1b and its corresponding circuit model is shown in Figure E2. The PCB under test is placed on an electrically floating induction plate. A dielectric foil separates the PCB from the plate. Capacitance of the PCB is set according to the required stress level by setting the correct thickness of the dielectric layer. Thin dielectric represents the highest CBE stress level for the PCB and a thicker dielectric can be used to adjust stress level to represent a real world situation. The induction plate is separated from the ground plane by a second dielectric plate. The induction plate capacitance can be adjusted according to the influence found in the process, or to evaluate a general level (as an example, four times higher than the PCB capacitance) by changing the area of the plate or thickness of the dielectric.

CBE stressing is carried out as follows. The PCB is placed on a thin dielectric foil and both the PCB and the induction plate are neutralized. Then a high voltage generator is used to apply a stress voltage on the floating induction plate. The induction plate will induce a potential on the PCB, and as soon as the potential stabilizes the voltage source is disconnected. The point discharge location of interest on the PCB is touched by a probe with a short grounding wire. Initial and residual potential of the induction plate is recorded before and after a discharge. Equations (1-4) are used to calculate discharge parameters and the stress level is given by Q_{mobile}, E_{ESD}, and stress voltage. In addition, $C_{induction}$, C_{PWB}, C_{ESD} and L values have to be given to validate the stress level. An oscilloscope can be used to measure the discharge current and transferred charge.

$$C_{ESD} = \frac{C_{Induction} \cdot V_{Initial} - C_{Induction} \cdot V_{\mathrm{Re}sidual}}{V_{Initial}} \quad (1)$$

$$Q_{Mobile} = C_{ESD} \cdot V_{Initial} \quad (2)$$

$$E_{ESD} = \frac{Q_{Mobile}^2}{2 \cdot C_{ESD}} \quad (3)$$

$$L = \frac{\left(\frac{1}{2\pi f_0}\right)^2}{C_{ESD}} \quad (4)$$

Where:

$V_{Initial}$ is a potential of the induction plate before the ESD event.

$V_{Residual}$ is a potential of the induction plate after the ESD event.

$C_{Induction}$ is a capacitance between the induction plate and a ground plane. C_{PCB} is a capacitance between discharge circuit of the PCB and the induction plate which can be measured.

C_{ESD} is a source capacitance of the discharge circuit, which consists of a serial capacitance $C_{induction}$ and C_{PCB}.

Q_{Mobile} is a transferable charge of the discharge circuit.

E_{ESD} is a calculated energy of the discharge. Inductance L is calculated from a resonant frequency when applicable.

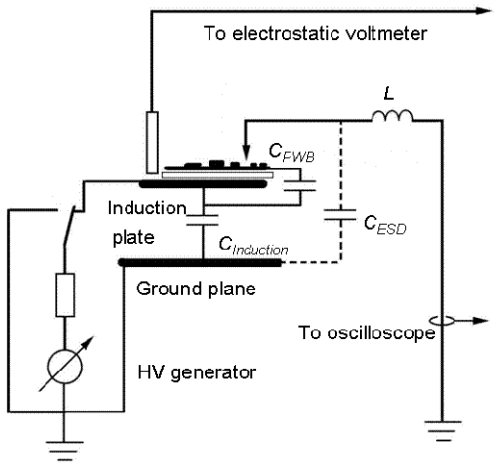

Figure E2: CBE method allowing variability in measuring CBE board risk to devices.

E.6 Charged Board Event Test Results

An example of the CBE discharge from the setup described in the previous section is shown in Table E-I. Discharge parameters are captured from a small PCB (size 40 mm X 100 mm) and a single PGA component (size 10 mm x 10 mm). Here the PCB represents the CBE discharge and the PGA gives the CDM parameters with the same setup. CBE discharge parameters depend on the electrostatic source circuit and discharge circuit. In this example, discharge was made through a 40mm long ground wire and a CT2 current probe was used to capture the discharge current. Measured discharges are presented in Figure E3 and the discharge circuit parameters in Table E-I.

Table E-I. Source circuit parameters and calculated discharge parameters

Stress Level	$C_{Induction}$ [pF]	C_{PWB} [pF]	C_{ESD} [pF]	$V_{Initial}$ +/- [V]	$V_{Residual}$ +/- [V]	L_{Stray} [nH]	Q_{Mobile} [nC]	$E_{Potential}$ [uJ]
CBE	89	33	24	1024	748	< 30	25	13
CDM	89	3	3	1024	995	< 30	2.6	1.3

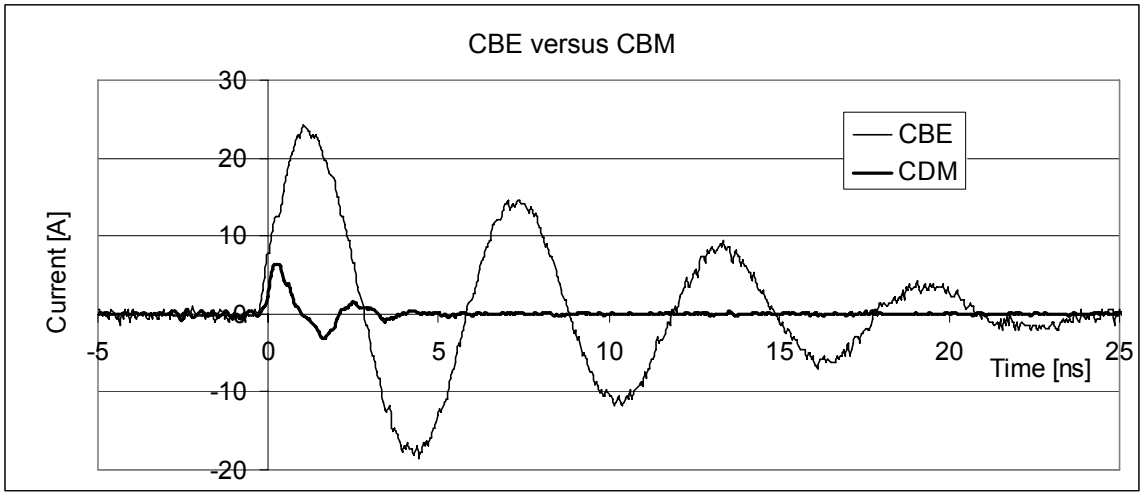

Figure E3: Comparison of CBE and CDM discharges from the CBE discharge setup.

Returning to the CBE test setup in [6], Figure E4 compares the CDM discharge waveform for a single Digital Signal Processor (DSP) IC to the charged board waveform for the same DSP device mounted to a customer return PCB shown in Figure E1a. Not surprisingly, for a given charge voltage (250V in this case), the CBE discharge has much higher peak current than the CDM discharge. This is because the PCB capacitance is much higher than IC package capacitance. Also, the CBE event has a faster rise time than the corresponding CDM event. This is because the inductance of the discharge path in this case is lower on the PCB than on the stand-alone DSP device. This was primarily because the traces on the measured PCB are much wider and thicker than bond wires on an IC, which is generally the case. The net result of the much higher peak current / faster waveform rise time for the PCB is that a given IC that is effectively immune to ESD damage at the device-level may be quite susceptible to ESD damage at the board level. If the mounted IC is in the primary discharge path on the PCB, the CBE ESD damage on the IC will be much more severe. Consequently, such ESD damage can look like EOS damage.

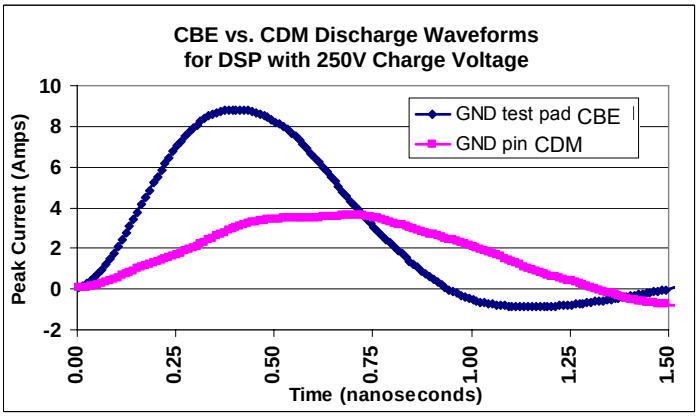

Figure E4: Comparison of CBE vs. CDM discharge waveforms.

E.7 Identifying and Minimizing Charged Board Event (CBE) Failures

ICs are most susceptible to CBE ESD damage if one or more of the following conditions apply:

1. The IC is adjacent to large insulators such as plastic sockets, plastic covers or plastic connectors that can develop a charge.
2. The IC is close to PCB edges, especially PCB edge connectors, mounting holes, or test points.
3. The IC has numerous supply / ground pins that are soldered to board supply / ground planes, especially if the board supply / ground planes are large relative to the IC.
4. The IC has a large die that results in a very low impedance discharge path, especially if the IC is the primary discharge path for the PCB.
5. The PCB does not include explicit EOS/ESD protection such as Transient Voltage Suppressors and Schottky diodes across the supply planes.

ICs and other components on PCBs are most susceptible to CBE ESD damage during the processing steps from when they are first populated with components until they are inserted into a case or other enclosure that provides adequate ESD protection. Balanced ionizers should be used throughout PCB manufacturing lines to minimize PCB charging, particularly during steps when insulating components (sockets, connectors, etc.) are mounted, and just prior to convection/IR reflowing or wave soldering. This is also supported by a case study in CDM Control, Chapter 3 (Section 3.2.2) of this document.

Also, it is a design mistake if a connector is designed so that an I/O pin can make the first electrical connection. Typically it is the ground pin or EMC shield around the connector that must make the first contact.

CBE sensitivity is a function of the board size / layout, charging potential of the board / materials used on the board, and particular assembly steps. A particular CBE test setup cannot duplicate all possible scenarios of CBE discharge. The measured peak current is also a function of where on the board the current is measured. CBE sensitivity analysis is best suited to individual applications; where the particular combination of CBE conditions can lead to assessments of CDM withstand voltages needed for the particular application.

Adherence to a certified ESD control program such as S20.20 from the ESD Association when assembling or handling circuit boards and installation of boards into systems can help prevent such failures from occurring [8]. However, it does not guarantee that CDM / CBE failures will not occur. For example, an assembly step of pulling protective tape from a LCD screen and subsequent assembly of the LCD onto a PCB may only take a second or two, not long enough for a balanced ionizer to remove the developed charge from the LCD.

E.8 Summary

Charged Board Event ESD is not as well documented as other ESD models but they represent a major real-world ESD threat in electronics system-level manufacturing. Even if all the individual components used for a given PCB have high device-level ESD robustness, one or more of these components may be very susceptible to ESD damage after mounting to a PCB. Since a PCB has much higher capacitance than an individual device, CBE damage can be much more severe than CDM damage. Therefore, before attributing an IC failure on a PCB to EOS, the possibility of charged board ESD damage should be explored. Adherence to a certified ESD control program, such as S20.20 from the ESD Association when assembling or handling circuit boards and installing boards into systems can help prevent such failures from occurring, but further analysis of the manufacturing environment is critical to understand development of charge / subsequent rapid discharge of boards.

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Revision History

Revision	Changes	Date of Release
1.0	Original release	March 2009
2.0	Grammer corrected throughout. Technical corrections in Appendix A, B and D.	April 2010